Intel 430VX PCIset Design Guide

June, 1997

TABLE OF CONTENTS

1

Overview

CHAPTER 1
OVERVIEW

Today's technology does not meet tomorrow's needs. With new applications such as multimedia, video conferencing, and on-line services; market requirements for the volume desktop computer will be higher performance, increased ease of use, and more features—all at a lower system price. The Intel 430VX PCIset (430VX) redefines the mainstream PC by providing new performance, features, and support for emerging technologies. The 430VX architecture maximizes PCI performance which allows for new performance levels, optimized multimedia support, and Plug and Play (PnP) support. A design based on a Pentium® processor Flexible Motherboard reduces time to market and minimizes cost to support upgradability and flexibility.

The information provided in this design guide is based on a reference platform developed around the Intel 430VX PCIset and the latest members of the Pentium processor family. Section 8.0 shows the schematics, jumper settings, component placement, and bill of materials. In addition to the reference motherboard board design, Section 9.0 provides an example of an SDRAM design.

A block diagram of the motherboard design is shown in Figure 1-1. A list of the motherboard design features is shown below.

- **CPUs Supported**
  - **Pentium® Processors at iCOMP® Index 1308\166 MHz Through iCOMP Index 610\75 MHz**
  - **Future Pentium Overdrive® Processors**
  - **Future High Performance Pentium Processors**
- **PCIset**
  - **82437VX System Controller (TVX)**
  - **82438VX Data Path (2 TDXs)**
  - **82371SB PCI ISA/IDE Xcelerator (PIIX3)**
- **SMBA Graphics Controller**
- **DRAM Main Memory**
  - **4 DRAM SIMM Sockets for Support for 4 MB to 128 MB at 60 ns or 70 ns (3V or 5V)**
  - **EDO DRAM or Fast Page Mode DRAM**
- **L2 Cache SRAM**
  - **3.3V Pipelined Burst SRAMs**
  - **Supports 256 KB of Direct-Mapped, Writeback Second Level Cache**
- **PCI ISA/IDE Xcelerator**
  - **Integrated Fast IDE Interface**
  - **Support for up to 4 Devices**
  - **PIO Mode 4 Transfers Up to 16 MB/s**
  - **Integrated 8x32 Bit Buffer for PCI IDE Bus Master Burst Transfers**
- **USB ready**
- **Slots**
  - **3 PCI**
  - **3 ISA**
- **3.3V Clock Driver**
- **Form Factor**
  - **2/3 Baby AT**
- **Number of Board Layers**
  - **4 (2 signal layers)**
- **Socket 5 (Socket 7 ready)**
- **Flash Device**
  - **1-Mbit Flash Implementation**
  - **Provides Upgrade to 2-Mbit Flash**

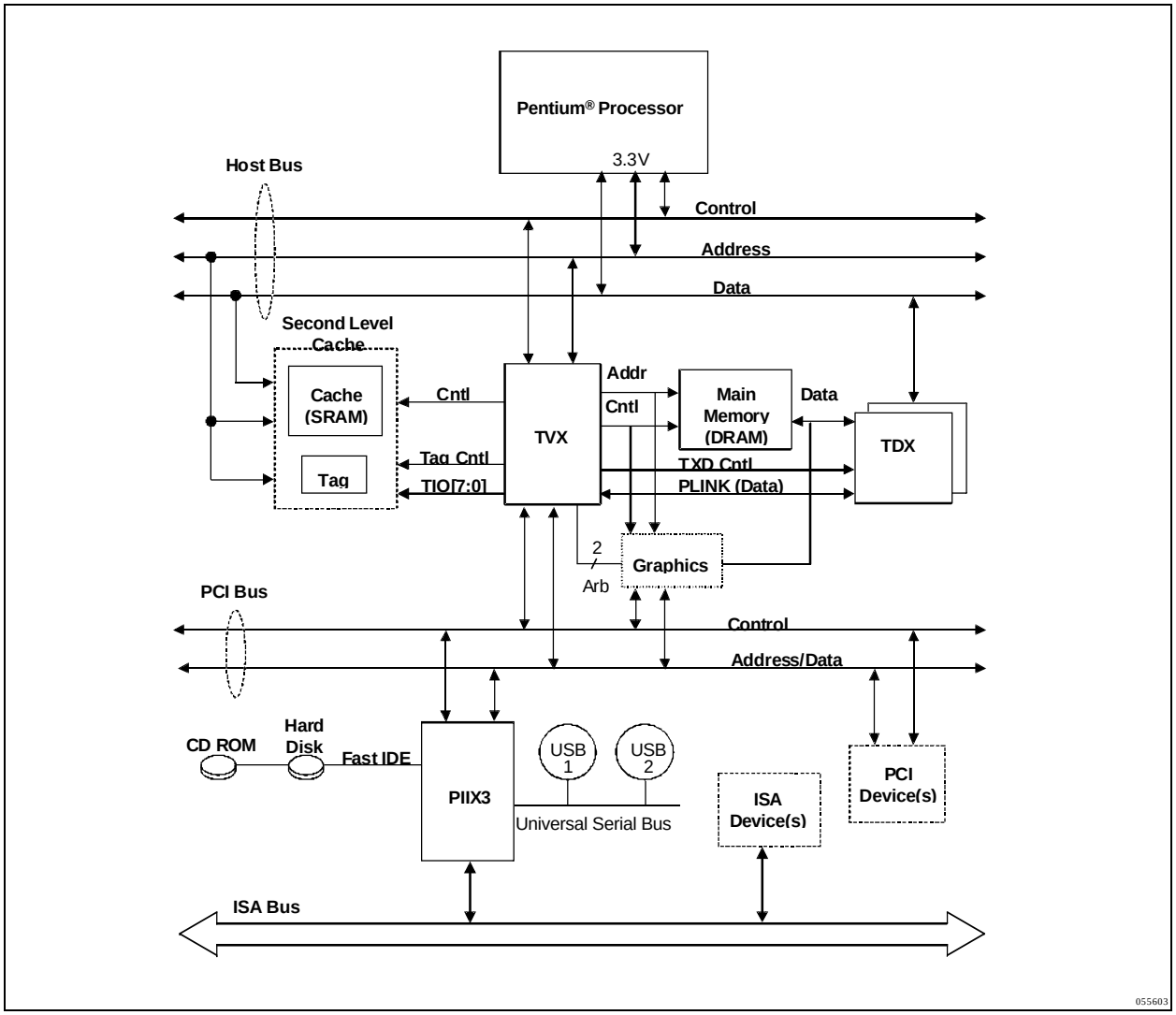


Figure 1-1. Intel 430VX PCIset System Block Diagram

1.1 Intel 430VX PCIset

The Intel 430VX PCIset (430VX) (Figure 1-1) consists of the 82437VX System Controller (TVX), two 82438VX Data Path (TDX) units, and the 82371SB PCI I/O IDE Xcelerator (PIIX3). The TVX and two TDXs form a Host-to-PCI bridge. The PIIX3 is a multi-function PCI device providing a PCI-to-ISA bridge, a fast IDE interface, an APIC interface, and a host/hub controller for the Universal Serial Bus (USB). The PIIX3 also provides power management.

The two TDXs provide a 64-bit data path to the host and to main memory and provide a 16-bit data path (PLINK) between the TVX and TDX. The PLINK provides the data path for CPU to PCI accesses and for PCI to main memory accesses. The TVX and TDX bus interfaces are designed for 3V and 5V busses. The 430VX connects directly to the Pentium processor 3V host bus; the 430VX connects directly to 5V or 3V main memory DRAMs; and the TVX connects directly to the 5V PCI Bus.

The TVX and TDX interface with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus. The 430VX implements a Shared Memory Buffer Architecture (SMBA) handshake 2-wire protocol that allows a graphics controller to use a portion of system memory as its frame buffer region. In addition, the PLINK bus is used to connect the PCI bus with the TDX, through the TVX (see Figure 1-1).

DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard Page Mode (SPM), Extended Data Out (EDO), and Synchronous DRAM (SDRAM) memory. The DRAM interface supports 4 Mbytes to 128 Mbytes of system memory with five RAS lines and also supports symmetrical and asymmetrical addressing for 512Kx32, 1Mx32, 2Mx32, and 4Mx32 deep SIMM modules (single- and double-sided). The TVX supports SDRAM 1Mx64, 2Mx64, and 4Mx64 deep DIMM modules (asymmetrical single- and double-sided). The 430VX requires that x32 and x64 SIMMs/DIMMs be used.

Second-Level Cache

The TVX supports a write-back cache policy providing all necessary snoop functions and inquire cycles. The second-level cache is direct mapped and supports both a 256-Kbyte or 512-Kbyte SRAM configuration using either pipelined burst or standard SRAMs. Pipeline burst configuration performance is 3-1-1-1 for read/write cycles; pipelined back-to-back reads can maintain a 3-1-1-1-1-1-1-1 transfer rate.

TDX

Two TDXs create a 64-bit CPU memory data path. The TDXs also interface to the 16-bit PLINK inter-chip bus on the TVX for PCI transactions. The combination of the 64-bit memory path and the 16-bit PLINK bus make the TDXs a cost effective solution, providing optimal CPU-to-main memory performance, while maintaining a small package footprint (100 pins each).

PCI Interface

The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX3 bus master requests. The TVX and TDXs together provide the interface between PCI and main memory; however, only the TVX connects to the PCI bus.

The PIIX3 incorporates a fully PCI Bus compatible master and slave interface. As a PCI master, the PIIX3 runs cycles on behalf of DMA, ISA masters, or a bus master IDE. As a PCI slave, the PIIX3 accepts cycles initiated by PCI masters targeted for the PIIX3's internal register set or the ISA bus. The PIIX3 directly supports the PCI interface running at either 25 MHz, 30 MHz, or 33 MHz.

ISA Interface

PIIX3 incorporates a fully ISA Bus compatible master and slave interface. PIIX3 directly drives five ISA slots without external data buffers. External transceivers are used on the SA[19:8] and SBHE# signals to permit these signals to be used with the IDE interface. The ISA interface also provides byte swap logic, I/O recovery support, wait state generation, and SYSCLK generation.

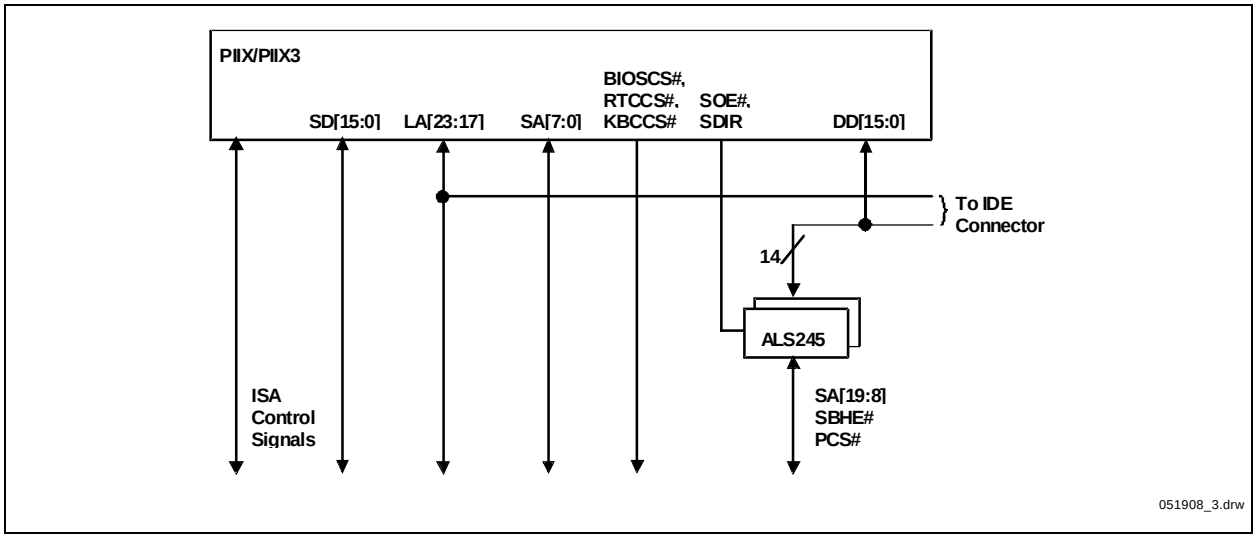


Figure 1-2. ISA Interface

DMA Interface

The DMA circuitry incorporates the functionality of two 82C37 DMA controllers with seven independently programmable channels (Channels 0-3 and Channels 5-7). DMA Channel 4 is used to cascade the two controllers and defaults to cascade mode in the DMA Channel Mode (DCM) Register.

Each DMA channel is hardwired to the compatible settings for DMA device size; channels [3:0] are hardwired to 8-bit count-by-bytes transfers and channels [7:5] are hardwired to 16-bit count-by-words (address shifted) transfers. The PIIX3 provides the timing control and data size translation necessary for the DMA transfer between the memory (ISA or main memory) and the ISA Bus device. ISA Compatible and type F DMA timings are supported. PIIX3 provides 24-bit addressing in compliance with the ISA-Compatible specification.

PIIX3 integrates a high performance interface from PCI to IDE. This interface is capable of accelerated PIO data transfers as well as acting as a PCI Bus master on behalf of an IDE DMA slave device. PIIX3 provides an interface for both primary and secondary IDE connectors.

Universal Serial Bus

PIIX3 contains a USB Host Controller (HC). The Host Controller includes the root hub with two USB ports. This permits connection of two USB peripheral devices directly to the PIIX3 without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The USB's PCI configuration registers are located in function 2, PCI configuration space. The PIIX3 Host Controller completely supports the standard Universal Host Controller Interface (UHCI) and thus, takes advantage of the standard software drivers written to be compatible with UHCI.

Interval Timer

PIIX3 contains three counters that are equivalent to those found in the 82C54 programmable interval timer. The three counters are contained in one PIIX3 timer unit, referred to as Timer-1. Each counter output provides a key system function. Counter 0 is connected to interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker. The 14.31818 MHz counters normally use OSC as a clock source.

Interrupt Controller

PIIX3 provides an ISA compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded so that 13 external and three internal interrupts are possible. The master interrupt controller provides IRQ[7:0] and the slave interrupt controller provides IRQ[15:8]. The three internal interrupts are used for internal functions only and are not available to the user. IRQ2 is used to cascade the two controllers together. IRQ0 is used as a system timer interrupt and is tied to Interval Timer 1, Counter 0. IRQ13 is connected internally to FERR#. The remaining 13 interrupt lines (IRQ[15,14,12:3,1]) are available for external system interrupts. Edge or level sense selection is programmable on an individual channel by channel basis.

The Interrupt unit also supports interrupt steering. PIIX3 can be programmed to allow the four PCI active low interrupts (PIRQ[D:A]#) to be internally routed to one of 11 interrupts (IRQ[15,14,12:9,7:3]). In addition, the motherboard interrupt (MIRQ0) may be routed to any of the 11 interrupts.

Stand-Alone I/O APIC Support

The PIIX3 supports a stand-alone I/O APIC device on the ISA X-Bus. PIIX3 provides a chip select signal (APICCS#) for the I/O APIC. It also provides handshake signals to maintain buffer coherency in the I/O APIC environment.

X-Bus Peripheral Support

PIIX3 provides positive decode (chip selects) and X-Bus buffer control (XDIR# and XOE#) for a real time clock, keyboard controller and BIOS for PCI and ISA initiated cycles. PIIX3 also generates RTCALE (address latch enable) for the RTC. The chip selects are generated combinatorially from the ISA SA(16:0) and LA(23:17) address lines (Note that it is assumed that ISA masters drive SA(19:16) and LA(23:17) low when accessing I/O devices). PIIX3 also provides PS/2 mouse support via the IRQ12/M signal and coprocessor functions (FERR# and IGNNE#). Software can enable or disable the chip selects and X-Bus buffer control lines.

Coprocessor Error Function

This function provides coprocessor error support for the CPU. FERR# is tied directly to the coprocessor error signal of the CPU. If FERR# is driven active to the PIIX3, an internal IRQ13 is generated and the INTR output from the PIIX3 is driven active. When a write to I/O location F0h is detected, PIIX3 negates IRQ13 (internal to the PIIX) and drives IGNNE# active. IGNNE# remains active until FERR# is driven inactive. Note, that IGNNE# is not driven active unless FERR# is active.

Mouse Function

When the mouse interrupt function is enabled, the mouse interrupt function is provided on the IRQ12/M input signal. In this mode, a mouse interrupt generates an interrupt through IRQ12 to the Host CPU. PIIX3 informs the CPU of this interrupt via an INTR.

Power Management

PIIX3 has extensive power management capability permitting a system to operate in a low power state without being powered down. In a typical desktop personal computer there are two states—Power-On and Power-Off. Leaving a system powered on when not in use wastes power. PIIX3 provides a Fast On/Off feature that creates a third state called Fast Off. When in the Fast Off state, the system consumes less power than the Power-On state.

The PIIX3's power management architecture is based on three functions—System Management Mode (SMM), Clock Control, and Advanced Power Management (APM). Software (called SMM code) controls the transitions between the Power-On state and the Fast Off state. PIIX3 invokes this software by generating an SMI to the CPU (asserting the SMI# signal). A variety of programmable events are provided that can generate an SMI. The SMM code places the system in either the Power-On state or the Fast Off state.

1.1.1 82437VX TVX and 82438VX TDX Features

- **Supports All 3V Pentium Processors at 66 MHz, 60 MHz, and 50 MHz**
- **PCI 2.1 Compliant**
- **Integrated DRAM Controller**
  - **64-bit Path to Memory**
  - **Mbytes to 128 Mbytes of Main Memory**
  - **Supports Mixed Memory Technologies (EDO/SPM/SDRAM)**
  - **EDO/Fast Page Mode DRAM Support (6-2-2-2 Reads at 66 MHz)**
  - **SDRAM (1-1-1 at 66 MHz)**
  - **5 RAS Lines Support for Symmetrical and Asymmetrical DRAMs**
  - **QWord Deep Buffer for 3-1-1-1 Posted Writes, and DWord and Burst Merging**
  - **Supports 3V or 5V DRAMs**
  - **External Buffers on MA Lines Are Not Required**
- **Integrated Second-Level Cache Controller**
  - **Direct Mapped Organization**
  - **Supports 256K and 512K Pipelined Burst, and Standard SRAM**
  - **Cache Hit Read/Write Cycle Timings at 3-1-1-1 with Burst SRAM**
  - **Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1**
  - **Supports Write Back**
- **Fully Synchronous 25/30/33-MHz PCI Bus Interface**
  - **5 PCI Bus Masters (Including PIIX3)**
  - **Converts Back-to-Back Sequential PCI Memory Writes to PCI Burst Writes**
  - **CPU-to-PCI Memory Writes Posting with 5-DWord Deep Buffers**
  - **PCI-to-DRAM Read Prefetching (5 QWords)**
  - **PCI-to-DRAM Posting (18 DWords)**
  - **Multi-Transaction Timer to Support Multiple Short PCI Transactions**
- **Shared Memory Buffer Architecture (SMBA) Support:**
  - **Supports Graphics Controller through a Two-Wire Protocol**
  - **Enhanced Performance Features Specific to SMBA**
- **Supports the Universal Serial Bus (PIIX3)**
- **208-Pin QFP System Controller (TVX), two 100-Pin QFP Data Paths (TDX)**

The Intel 430VX PCIset (430VX) consists of the 82437VX System Controller (TVX), two 82438VX Data Path Units (TDX), and the 82371SB PCI I/O ISA IDE Xcelerator (PIIX3). The PCIset forms a Host-to-PCI bridge, and provides the second-level cache control and a full function 64-bit data path to main memory. The TVX integrates the cache and main memory DRAM control functions and provides bus control for transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with either standard or pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the TVX's DRAM controller, five rows are supported providing up to 128 Mbytes of main memory. A Shared Memory Buffer Architecture (SMBA) 2-wire interface allows a graphics controller to use an area of system memory as its frame buffer. The 430VX has been enhanced through additional buffers, programmable timers, burst and DWord merging, and optimized DRAM timings to maintain a high level of performance when used in an SMBA environment. The TDXs provide the data paths between the CPU/cache, main memory, and PCI. For increased system performance, the TDXs contain read prefetch and posted write buffers.

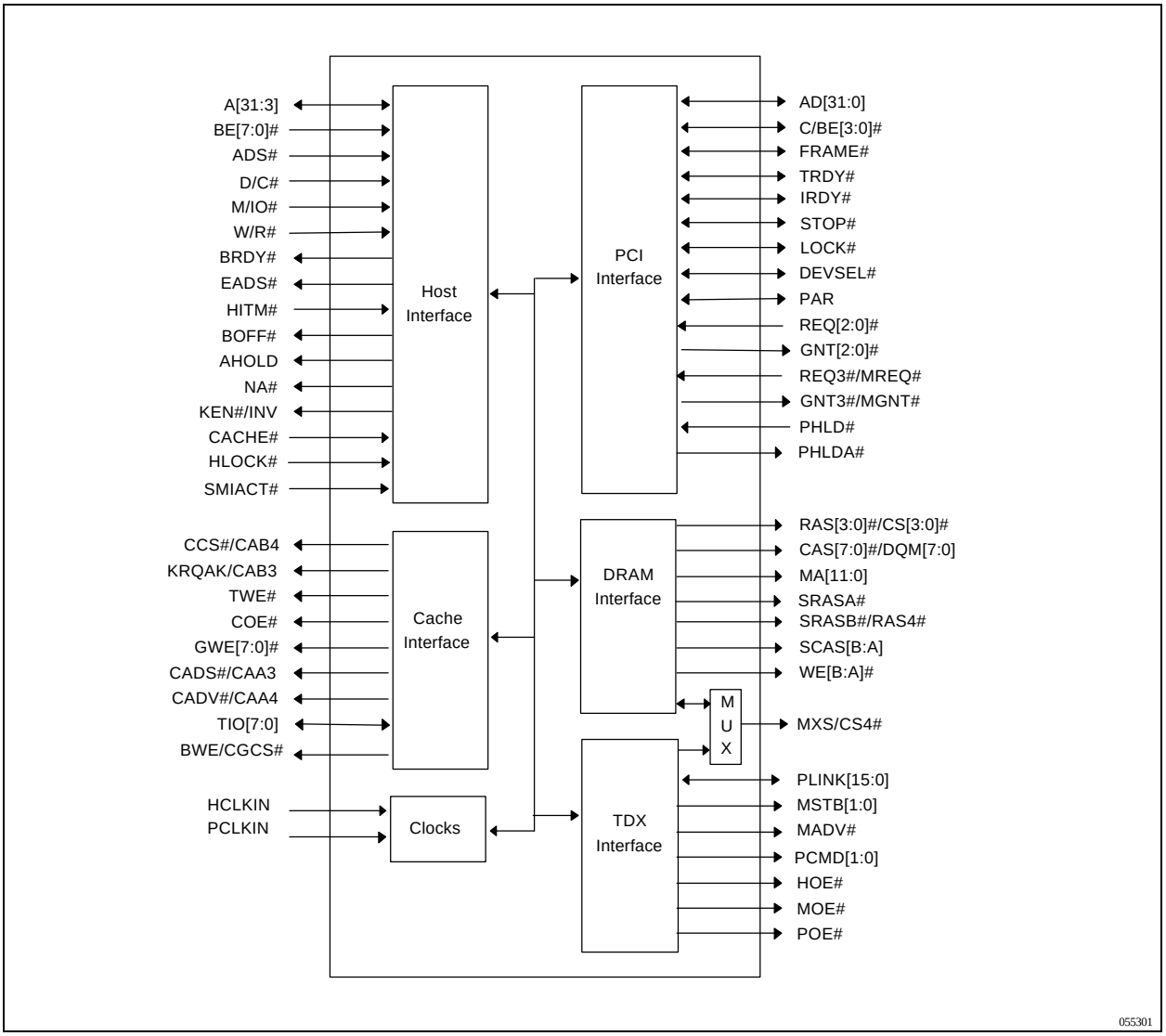


Figure 1-3. TVX Simplified Block Diagram

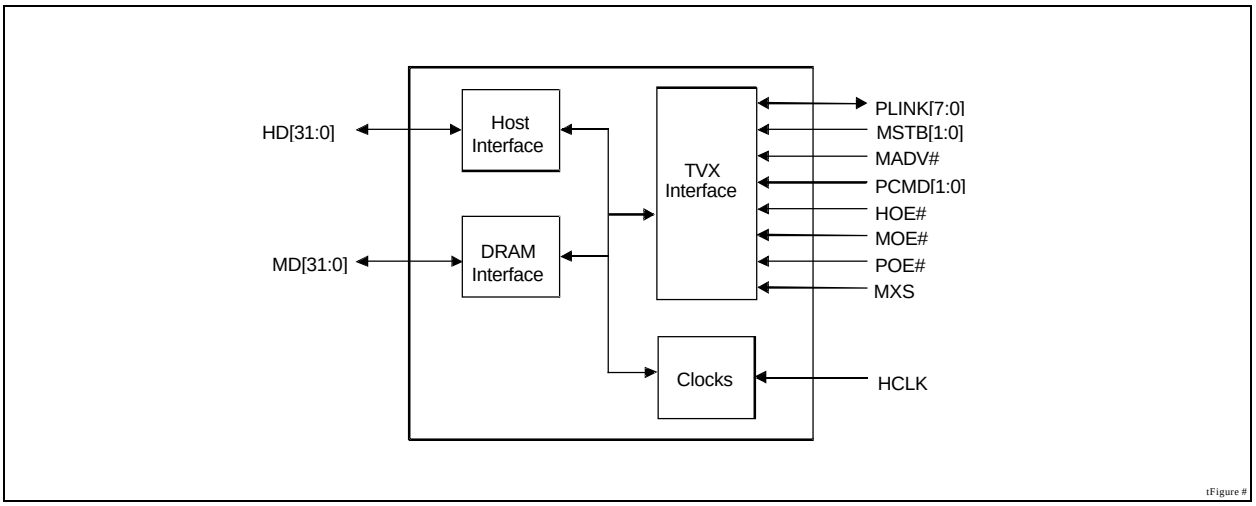


Figure 1-4. TDX Simplified Block Diagram

1.1.2 82371SB PIIX3 Features

- **Bridge Between the PCI Bus and ISA Bus**
- **Universal Serial Bus (USB) Host Controller**
  - **Compatible With Universal Host Controller Interface (UHCI)**
  - **Contains Root Hub With Two USB Ports**
- **PCI Specification Revision 2.1 Compliant**
- **PCI and ISA Master/Slave Interface**
  - **PCI from 25–33 MHz**
  - **ISA from 7.5–8.33 MHz**
  - **5 ISA Slots**
- **Fast IDE Interface**
  - **Supports PIO and Bus Master IDE**
  - **Supports up to Mode 4 Timings**
  - **Transfer Rates to 22 Mbytes/Sec**
  - **Separate Master/Slave IDE Mode Support**
- **Plug-n-Play Port for Motherboard Devices**
  - **1 Steerable Interrupt Line**
  - **1 Programmable Chip Select**
- **Steerable PCI Interrupts for PCI Device Plug-n-Play**
- **Functionality of 1 82C54 Timer**
  - **System Timer; Refresh Request; Speaker Tone Output**
- **2 82C59 Interrupt Controller Functions**
  - **14 Interrupts Supported**
  - **Independently Programmable for Edge/Level Sensitivity**
- **Enhanced DMA Functions**
  - **2 8237 DMA Controllers**
  - **Fast Type F DMA**
  - **Compatible DMA Transfers**
  - **7 Independently Programmable Channels**
- **X-Bus Peripheral Support**
  - **Chip Select Decode**
  - **Controls Lower X-Bus Data Byte Transceiver**
- **I/O Advanced Programmable Interrupt Controller (IO APIC) Support**
- **System Power Management (Intel SMM Support)**
  - **Programmable System Management Interrupt (SMI)—Hardware Events, Software Events, EXTSMI#**
  - **Programmable CPU Clock Control (STPCLK#)**
  - **Fast On/Off Mode**
- **Non-Maskable Interrupts (NMI)**
  - **PCI System Error Reporting**
- **NAND Tree for Board-Level ATE Testing**
- **208-Pin QFP**

The 82371SB PCI I/O IDE Xcelerator (PIIX3) is a multi-function PCI device implementing a PCI-to-ISA bridge function and a PCI IDE function. In addition, the PIIX3 implements a Universal Serial Bus host/hub function. As a PCI-to-ISA bridge, the PIIX3 integrates many common I/O functions found in ISA-based PC systems—a seven channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and power management support. In addition to compatible transfers, each DMA channel supports type F transfers. Chip select decoding is provided for BIOS, real time clock, and keyboard controller. Edge/Level interrupts and interrupt steering are supported for PCI plug-and-play compatibility. The PIIX3 supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. The PIIX3 provides motherboard plug-and-play compatibility. The PIIX3 implements one steerable interrupt line and a programmable chip select. The interrupt line can be routed to any of the available ISA interrupts. The PIIX3 also provides support for an external I/O APIC.

The PIIX3 contains a Universal Serial Bus (USB) Host Controller that is UHCI compatible. The Host Controller moves data between system memory and devices on USB by processing data structures set up by the Host Controller Driver (HCD) software and generating the transaction on USB. Optimized partitioning between software and hardware operations maximizes performance and maintains flexibility. The Host Controller's PCI Bus master capability permits high performance data transfers to system memory. The Host Controller's root hub has two programmable USB ports.

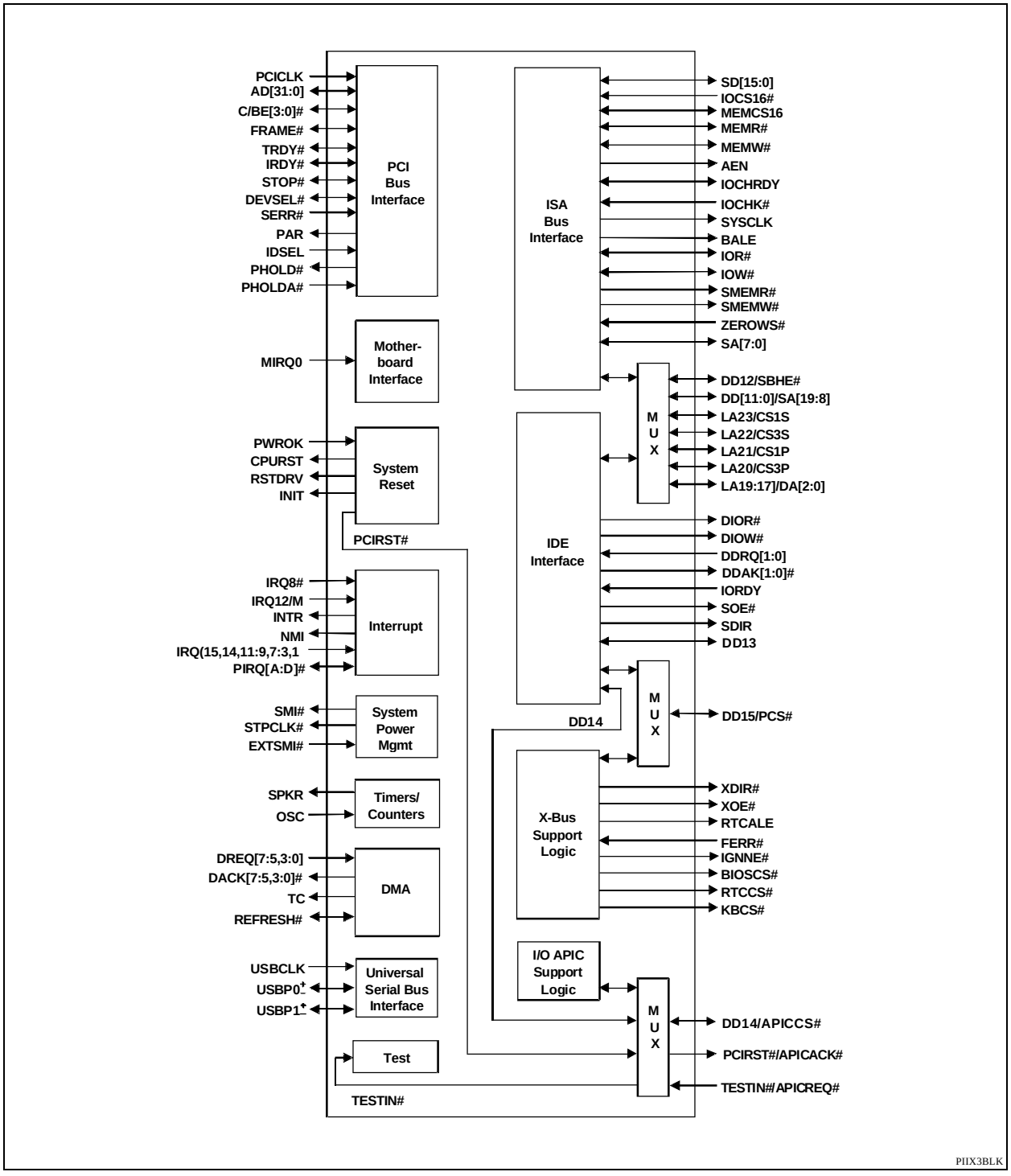


Figure 1-5. PIIX3 Simplified Block Diagram

2

Flexible Motherboard Design Layout Review Checklist

CHAPTER 2
FLEXIBLE MOTHERBOARD DESIGN LAYOUT REVIEW CHECKLIST

2.1 Basic Connectivity

- **V_{SS} pins:**
  - 53 V_{SS} pins all connected to ground plane in 296-pin LIF socket
  - 68 V_{SS} pins all connected to ground plane in Socket 7
- **$V_{CC}2$ pins:**
  - 25 $V_{CC}2$ pins all connected to core power plane in 296-pin LIF socket
  - 28 $V_{CC}2$ pins all connected to core power plane in Socket 7
- **$V_{CC}3$ pins:**
  - 28 $V_{CC}3$ pins all connected to I/O power plane in 296-pin LIF socket
  - 32 $V_{CC}3$ pins all connected to I/O power plane in Socket 7
- **NC/INC:**
  - 14 NC/INC pins all unconnected in 296-pin LIF socket
  - 14 NC/INC pins all unconnected in Socket 7
- **5V pins:**
  - $V_{CC}5$ pins (AN01, AN03) connected to 5V in Socket 7

2.2 General Layout Checks

- **Split plane:**
  - Power planes are split into $V_{CC}2$ and $V_{CC}3$ around the CPU
- **$V_{CC}2$ plane:**
  - $V_{CC}2$ plane extends ~0.5” from CPU power pins, not routed only through the PGA pin field
- **Good power plane routing especially for $V_{CC}2$:**
  - Avoid narrow/long routing to minimize voltage drop
  - Avoid an excessive number of vias that restrict current flow in narrow power routes
- **Power for other 3.3V components (PCIset, cache, clock driver, etc.):**
  - Same power plane as CPU $V_{CC}3$ is recommended
- **Clock:**
  - Route on the layer nearest the ground layer so as not to cross multiple power island gaps
- **1.0 µF caps:**
  - Placed near CPU $V_{CC}2$ pins with minimum trace length to power plane vias. Placement around the socket periphery near the majority of power pins first, then use socket cavity if necessary
- **100 µF caps:**
  - Placement near CPU $V_{CC}2$ pins

- **0.1 µF caps from $V_{CC}3$ to V_{SS}:**

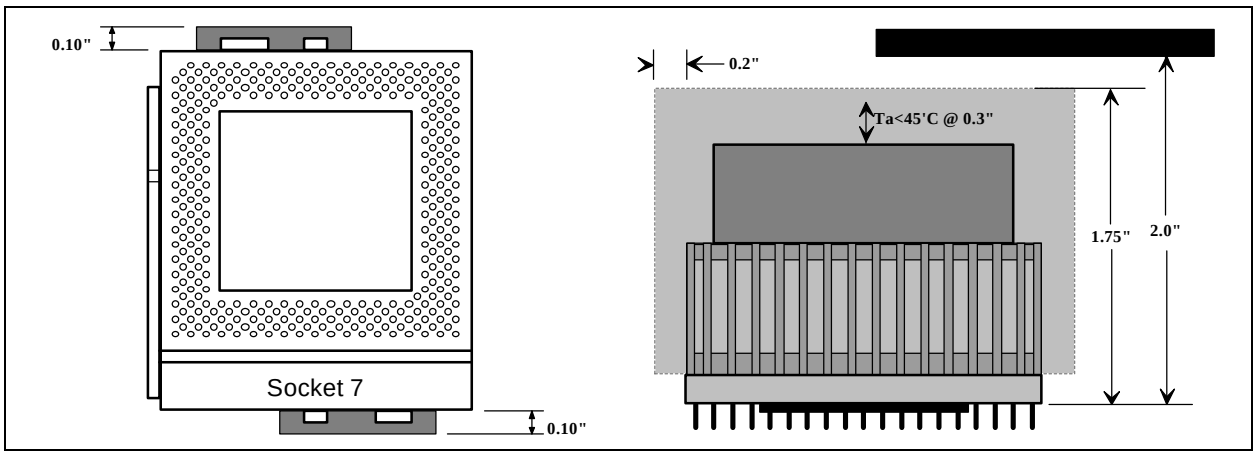
— Placement near $V_{CC}3$ pins

- **0.1 µF caps from $V_{CC}2$ to $V_{CC}3$:**
  — It is recommended to place caps between $V_{CC}2$ and $V_{CC}3$ planes near high speed signals (clock, data, and low address lines) that cross the power island gaps

Refer to the Pentium Processor Flexible Motherboard Design document for additional design considerations.

2.3 Socket Mechanical Requirements

- Physical space requirements for Socket 7 must be met
  — 0.1” keep-out zones met for Socket 7heatsink clip tab clearance
  — 1.75” total space above socket
  — 0.2” space from all four sides of the package
  — 2.0” total space above Socket 7 to immovable objects

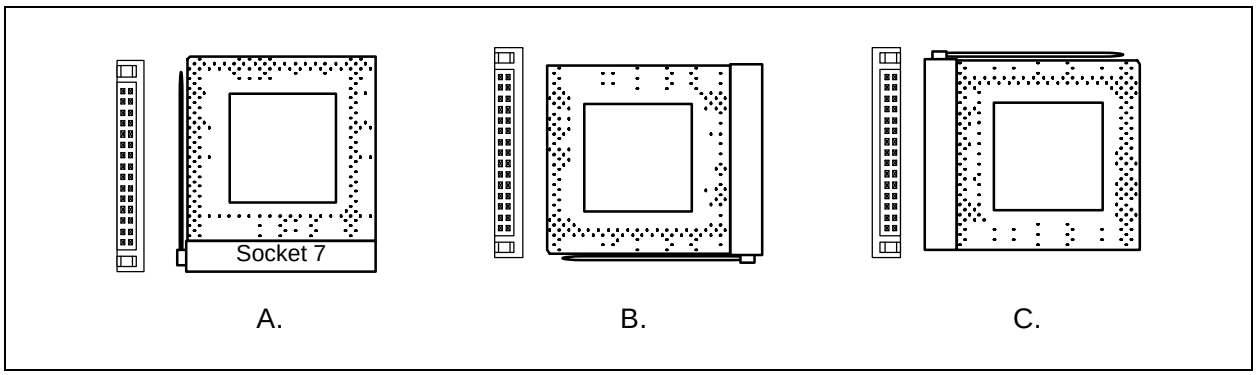


2.4 Socket Thermals Requirements

- **Fan:**
  — Power supply fan only
  — Additional system fan will be used
- **Path:**
  — Verify airflow to CPU is not obstructed
- **Power dissipation**
  — Socket 7 requirement is 17W

2.5 Header 7/VRM

- **Placement:**
  - Header 7 within 1” of CPU $V_{CC}2$ pins (may be further but may experience excessive resistance in power plane)
- **The physical space requirements of Voltage Regulator Module 7 have been met:**
  - 1.48” total space for VRM/Header 7 from motherboard
  - 0.5” maximum component space on front of VRM PCB (heatsink side)
  - 0.238” maximum component space on back of VRM PCB (component side)
  - 2.6” maximum VRM PCB width
- **SENSE:**
  - Routed to a CPU $V_{CC}2$ pin or the center of the CPU core voltage island
- **Circle letter noting orientation of header and CPU socket in figure below:**



2.6 82430VX Design Checklist

The following checklist is a guide when designing or reviewing a board design that uses the 82430VX PCIset. The 82430VX is used in a Uni-Processor, ISA System and supports all 3V Pentium Processors.

2.6.1 CPU

- Refer to the "P55C/FMB Design Review Checklist," "Socket 7 Design Review Checklist," and "Socket 7 Specification" for additional information on CPU related requirements. The P55C/FMB and Socket 7 Design Review Checklists are available on Lotus Notes*.
- Drive Strength—The CPU sets its output buffers drive strength using the BRDYC# & BUSCHK# signals that are sampled at RESET. In an 82430VX system, a low drive setting is used, so these signals can be left as no connects. BRDYC# has an internal pullup that will default to a low drive buffer strength if not overridden at RESET.
- Frequency Selection—BF[1:0] pins on the processor should be supported to allow support for different speeds of Pentium Processor. The ability to pull both signals low is required to support the 150- & 166-MHz processors. BF[1:0] should be pulled low with 100 ohm (or less) resistors. Also, it is recommended that a 100 ohm (or less) resistor also be used to pullup the BF0 line to support future Pentium speed upgrades. Jumpers are recommended to support the above pull-up/pull-down options.
- V_{CC}2DET (P55C)—This signal can be used as a safeguard to prevent plugging in a P54C into a Socket set up for P55C support (2.5 Vcore). The P55C will always drive V_{CC}2DET low. This pin can be used in a flexible motherboard implementation to correctly set the voltage regulator to drive the correct V_{CC} to the CPU.
- ADSC# should be used to drive the cache subsystem, and ADS# should be used to drive the chipset. These signals are functionally identical to each other and two copies are provided by the processor for loading reasons.
- INV and KEN# should be tied together at the CPU. The 82430VX muxes these signals. KEN# is used during CPU read cycles and INV is used during L1 snoop cycles.
- Pullups (to 3V): FLUSH#, FRCMC#, WB/WT#, AP, & PEN#—8k2ohm.
- Pullups (to 3V): CPURST—330 ohm; SMI#, STPCLK#, INTR#, NMI, and IGNNE#—4.7K (These are open collector outputs from the PIIX3 component); HDP[7:0]—4.7K (these parity signals are not supported by the 82430VX).
- If open collector drivers are used to generate INIT and A20M#, pull up to 3.3V (330 ohm for INIT, 4.7 kohm for A20M#).
- The HOLD and EWBE# pins on the processor are tied to GND.
- No Connects: R/S#, TCK, TDI, TMS, TRST#, APCHK#, BP[3:0], HIT#, HLDA, IERR#, PCHK#, PRDY, PWT, PCD, SCYC, TDO, PICCLK, PICDO, PICD1, PHITM#, PHIT#, PBGNT#, CPUTYP, PBREQ#,U/O# (or D/P#), UPVRM(or KEY), BUSCHK#, BRDYC#, BREQ#.
- Split Core V_{CC}2 for P55C—The P55C requires two supply voltages; 2.5V±5% on its Vcore pins at about 3.0 Amps (166 MHz) required. Its external I/O pins operate at STDE (3.125–3.6V) levels and require 0.4A@166 MHz. Check the latest POR for confirmation.
- Unlike the Pentium Processor (735/90,815/100,1000/120, and 1110/133), these inputs on the P55C are not 5V tolerant: (CLK,PICCLK,AHOLD,BRDYC#,EADS#,KEN,WB/WT#,INV,NA#,EWBE#, BOFF#).
- Voltage—VRE to the socket allows the most flexibility to support the greatest number of processor types. To date, the highest current requirement is about 4.25 amps for the P54CS-166 and 5A for the P54CTB-200 OverDrive processor.

- V_{CC} and HCLK—The PP power-up specifications recommend that HCLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. Following this recommendation will ensure the long-term reliability of the processor.
- Decoupling—An appropriate quantity and quality of bypass decoupling capacitors are necessary for proper CPU operation. Proper conditioning of the voltage supplies to the CPU(s) will assure operation under worst case conditions. See the Pentium Processor Flexible Motherboard Design Guidelines document and Socket 7 Specification for guidelines for proper decoupling and Pinout requirements.

2.6.2 TVX and TDX Power-Up Requirements

- Power-up Protection—The TVX and TDX components require that one 100 ohm (at least .25 watt) and one 1.0 µF cap be connected in series to ground on the $REFV_{CC}5$ pins (pin 207 on the TVX and Pin 52 on the TDX's). One RC circuit is used for all three components (i.e the $REFV_{CC}5$ pins on all three devices are tied together).
- Bypass Capacitor for $V_{DD}5REF$ pins

  It is recommended to place a 0.01 µf (or greater capacitance) decoupling capacitor near as possible to each $V_{DD}5REF$ pin. The TVX has one $V_{DD}5REF$ pin (pin #207) and each TDX has one $V_{DD}5REF$ pin (pin# 52). These capacitors are not absolutely required, however it is recommended to keep noise to a minimum.

2.6.3 Host Interface

- A27 Strapping option—This TVX signal has a weak pulldown and should be pulled-up (with an external pull-up) for a host bus freq of 60 MHz, and left as a no connect for a host bus freq of 66 MHz. The inverted state of A27 at reset rising determines the DRAM refresh rate and host bus frequency for the TVX. The state is sampled and stored in DRAMC (57h) [0]. BIOS can use this bit to determine if the system is 60 MHz or 66 MHz.
- The Data byte lanes are arranged in an even/odd fashion on the TDX's, as shown in the 82430VX reference schematics.
- CPURST is used as the reset signal to the TVX.
- Internal Pulldowns: HD[63:0] on the TDX's have internal pulldowns. External pullups/pulldowns are not required.

2.6.4 L2 Cache

- GWE# and BWE#—The TVX only supports PBSRAM devices that use GWE# (global write enable—pin 16 on the TVX) and BWE# (pin 17 on the TVX). GWE# and BWE# must be connected from the TVX to each of thePBSRAMs.
- The Asynch cache implementation requires the use of external "AND" gates to gate the host BE#'s and the CGCS# signal (CGCS# is pin 17 on the TVX) to control the CS#'s on the SRAM. The gate is required to have a propagation delay of 8 ns or less at 66 MHz. There are also two copies of cache address 3 and 4 (CAB3, CAB4, CAA3, and CAA4) provided for loading purposes. CAB3 and CAA3 (similarly for CAB4 and CAA4) provide the same function and should be evenly distributed throughout the Asynch cache subsystem.
- Proper Speed Parts—Intel recommends the use of PBSRAMS with tco of 8.5 ns and cycle times of 15 ns, and 15 ns Tag, for operation at 66 MHz host bus frequencies. Intel recommends the use of 15 ns Asynch data SRAM and 15ns tag SRAM, for operation at 66 MHz host bus frequencies.
- Internal Pulldowns: TIO[7:0] on the TVX have internapulldowns.
- Host Bus Parity—82430VX does not support host bus parity so these signals are not used.
- Cache Type/Size Detection—Host addresses, A[31:28], are pulled either high or low and used by the TVX at RESET to determine the size and type of the L2 cache installed. The contents of the CC

register reflect the state at RESET and can be overwritten by BIOS. Note, if the BIOS that is being used can determine the L2 cache type and size, the external strapping resistors on A31–A28 are not required. The strapping requirements for the 82430VX are the same as the 82430FX. However, if the future cache is implemented, the strapping on the TVX KRQAK pin is still required.

- 512K PBURST support—A18 determines which bank is accessed. This address is connected to CE2 on the PBSRAMs of the lower bank and CE2# of the upper bank PBSRAMs.
- Coast Modules—If a COAST module is used, all recommendations and specifications contained in the "82430FX COAST specification (rev 1.x)" and the Flexible Cache Solution For the 82430VX and 82430HX PCIsets (Rev 2.x) should be followed. Both of these documents are available on Lotus Notes. In addition, **(1)** ECS2# and ECS1# on the COAST connector should be connected to gnd on the motherboard (for std Pburst cache support—assuming cache module is not used to upgrade a 256-Kb cache on the baseboard to 512 KB). **(2)** CALE on the COAST connector should be connected to $V_{CC}3$ on the motherboard (for Asynch cache support). **(3)** Motherboard presence detection circuitry (resistor network as shown in the COAST specification) is required on host address lines (HA28 through HA31) to allow the TVX to determine the COAST cache size/type.
- Future CACHE logic: The 82430VX provides an option for a future cache implementation. Additional logic (Inverter + several resistors and caps) is required to support this option. Refer to the cache pages in the reference schematics for information. Note: It is recommended that the inverter used to drive the future cache reset line be a 74HCT14 type device.

2.6.5 DRAM

- MA[11:0] and WE# Buffering—External buffering on the MA lines and WE# lines is not required, and must not be implemented. These lines must be connected directly to the DRAM. The TVX provides integrated programmable buffers on the MA lines, and two copies of WE# (WEA# and WEB#). The TVX also provides two copies of SRAS# (SRASA# and SRASB#) and SCAS# (SCASA# and SCASB#). Two copies of these signals were provided for loading reasons and should be evenly distributed throughout the DRAM subsystem. Using the 5th row of memory—Refer to the 82430VX EDS or datasheet for the recommended 5th ROW implementation. The 5th Row (i.e. RAS4 for EDO/FPM or CS4# for SDRAM) is limited to 8M's of memory (total), using 1Mx16 devices, and must be soldered down on the motherboard. If the 5th RAS line is used, all rows in the DRAM subsystem must be populated with all EDO/FPM or all DRAM. In a SDRAM five row system, MXS# on the TDX's must be pulled-up with a 1k resistor. Also, there is a restriction on the DRAM timings when 5 rows of memory are populated. At 66 MHz with 60 ns memory or 60 MHz with 70 ns memory, the burst rate must be set to X-3-3-3 EDO, x-4-4-4 FPM (register 58, bits [6:5] = '01h').
- Internal Pullups—MXS#/CS4#, CAS[7:0]#/DQM[7:0], WEB#, SRASB#/RAS4# on the TVX have internal pullups. External pullups are not required.
- Internal Pulldowns—CAB3 on the TVX, and MD[63:0] on the TDX's have internal pulldowns. External pullups/pulldowns are not required.
- Pin 46 on SIMM connector: Pin 46 on all SIMM connectors should be pulled to ground. This is an OE# for some SIMM module manufacturers.
- SDRAM—Refer to the latest Unbuffered Standard/SDRAM DIMM specification for the latest DIMM connector pinout. In addition, (1) The 82430VX supports unbuffered DIMM modules only. (2) Each DIMM requires two separate HCLKs to support double sided DIMMs. (3) Generally, only SDRAM and EDO come on DIMM's, however, the DIMM spec also specifies FPM. To support EDO/FPM on the same DIMM, OE0# (pin 31) and OE2# (pin 44) on the DIMM connector must be connected to ground on the motherboard, and WE2# (pin 48) must be connected to one of the TVX's Memory write enable signals (WEA# or WEB#). (4) Most SDRAM will be 3V only (i.e SDRAM I/O pins will not be 5V tolerant). When mixing and matching SDRAM with EDO/FPM, the EDO/FPM should also be 3V (i.e. receive and drive 3V levels).

- Series termination resistors—CAS[7:0]#/DQM[7:0] (10 ohm), RAS#[3:0]/CS#[3:0] (10 ohm), SRASB#/RAS4# (10 ohm—when used as RAS4#), MXS#/CS4# (10 ohm—when used as CS4#).
- Parity—The 82430VX does not support parity and requires that non-parity SIMMs and DIMMs be used. However, it is recommended that the parity pins on the DIMM and SIMM connectors be pulled-up to V_{CC} (3V or 5V, depending on the DRAM subsystem)—4.7k.

2.6.6 SMBA

- When designing in a SMBA graphics controller, the graphics vendor should review your graphics schematic pages for accuracy.
- PCIRST# should be tied to the Graphics device.
- REQ3#/MREQ# should be tied to 5V through a 10K resistor and GNT3#/MGNT# should be tied to 3V through a 10K resistor.
- In a SMBA design, the highest ROW (i.e ROW 4 in a four row design and ROW 5 in a five row design) is always populated. This is the ROW that the Graphics controller must drive. The Graphics controller only shares the "B" copy of the WEx# signals.
- The DRAM row assigned to the graphics controller, in a SMBA design, must be populated with EDO/SPM, only (i.e. SDRAM is not supported in the SMBA row). However, EDO/SPM and SDRAM can be mixed in a SMBA design, as long as the SMBA row is not populated with SDRAM.
- In a four DRAM Row SMBA system, if double sided SIMM sockets (EDO/FPM) are used on the motherboard, then the RAS3# (EDO/FPM) from the Graphics controller and TVX should be tied to the first bank of the double sided SIMM, and RAS2# (EDO/FPM) from the TVX, should be tied to the second bank of the double sided SIMM. This is required for supporting single sided SIMMs populated in the double sided SIMM sockets.

2.6.7 PCI

- Pullups (to 5V)—Resistors (2.7 kohm) on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, and REQ64# and ACK64# on PCI connectors. Resistors (10kohm) on REQ[3:0].
- Pullups (to 3V)—Resistors (10kohm) on GNT[3:0]#.
- PCI slots—82430VX supports up to four PCI masters in a non-SMBA system (with REQ[3:0]# and GNT[3:0]#), and three PCI masters in a SMBA system (with REQ[2:0]# and GNT[2:0]#). In this case, the REQ3# and GNT3# pair are used as the SMBA memory request (MREQ#) and SMBA memory grant (MGNT#) signals, respectively. Also, it is recommended, per the PCI spec, to place series resistors (~ 100 ohms) on each of the PCI connectors IDSEL lines.

2.6.8 ISA Bridge (PIIX3)

- PHLD and PHLDA: PHLDA—10K pullup to 3V, PHOLD—10K pullup to 5V.
- Pullups (to 5V): DD[12, 14, and 15—10K; The resistors should be placed on the system side of the 245 transceiver (i.e. not on the PIIX3 side).
- Pullups (to 3V): For signals connected to the Processor, refer to the CPU section.
- Pulldowns: DDRQ[1:0]—5.6K.
- SYSCLK strapping—The state of SYSCLK is sampled on the assertion of PWROK. To support both 50 MHz and 60/66 MHz on the host interface, a jumper, two 10k pullups, and an open collector buffer (e.g. 74F07) device is required to allow strapping for both 50 MHz and 60/66 MHz. One pullup is required to strap the PIIX3 for 50 MHz operation (divide by 3), and the buffer and second pullup is required to support 60/66 MHz operation (divide by 4). If 50 MHz alone is required, only a 10K pullup is required on SYSCLK. If 60/66 MHz alone is required, the buffer and one 10k pullup (on the output of the 74F07) is required. Refer to the reference schematics for implementation details. *Note: The PIIX3 can be strapped for (divide by 4), and BIOS can then*

write to bit 0, at register offset 6Ah, to set the divisor to 3 (50 MHz). In this case, the jumper and the pullup resistor (on the input side of the 74F07) used to strap the system for 50 MHz, can be removed. Also, this bit allows BIOS to change the divisor anytime after power-up.

- SD/XD transceiver—"A" side buffers point towards the ISA bus and "B" side buffers point towards the X-Bus.
- MASTER#—The PIIX3 doesn't require connection with the MASTER# signal from the ISA bus (same as the PIIX). Place a pull-up resistor (300 ohm) on MASTER# signal from ISA connectors.
- ISA Slots—The PIIX3 will support up to 5 ISA slots.
- 330 ohm pull-up resistor onRefresh# should be changed to 1k pull-up.

2.6.9 USB Interface

- Refer to the "82430VX Layout Recommendations document" for USB, clock, and general board layout recommendations.
- Pulldowns: USBPO+, USBPO-, USBP1+, USBP1- on PIIX3 outputs—(15k).
- $V_{CC}/V_{CC}3$ pin: Pin 130 provides the 3V interface for the USB. Tie to 3V. Also, place a .1 µf cap on this pin to gnd.
- USB Clock—48 MHz or 24 MHz with a duty cycle of better than 45/55% (24 MHz) or 40/60% (48 MHz) should be fed into the PIIX3's USB clock input, pin 146.
- The 30 ohm series termination resistors on the USBPx lines must be placed as close to the PIIX3 connector as possible.
- The 47 pf caps to ground on the USBPx lines must be placed on the PIIX3 side of the (30 ohm) series termination resistors.
- Ferrite beads and by-pass caps on power and ground are recommended for EMI purposes.

2.6.10 IDE Interface

- Refer to the "82430FX PCIset IDE Layout Guidelines rev 1.x" when implementing the IDE interface.
- Pull-up resistor on IORDY# (1kohm).
- Optional Pull-down resistor on pin 28 of the IDE connectors (470 ohm). It is recommended that PIN 28 be used as its newly defined operation, Per ATA rev2 spec: pin 28 is now defined as a cable select signal and should not be connected to BALE. The critical point with regard to pin 28 is: **do not** connect BALE to this pin. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable. The 430VX reference boards have 10K pull-ups on this line. The 10K pull-up still maintains compatibility with the standard hard drive master/slave configuration process (i.e. end-user setting the master/slave jumpers on the hard drive itself), and the pull-up does not prevent the IDE interface from functioning properly. However, if the OEM wants to take advantage of both the cable select master/slave configuration feature, and the standard master/slave configuration process, 470 ohm pull-downs can be placed on pin 28 of the IDE connectors.
- Primary IDE connector uses IRQ14 and the secondary IDE connector uses MIRQ0.
- All signals running to the two IDE connectors (except for IORDY#) have series terminating resistors (22–47 ohm). Refer to the "82430FX PCIset IDE Layout Guidelines, rev 1.x."
- DD0–15/SA transceivers hooked up correctly—DDs on the "A" side and SA's on the "B" side of a '245.
- Layout—Proper operation of the IDE circuit depends on the total length of the IDE bus. Follow the recommendations in our IDE Guidelines App Note carefully. The total signal length from the IDE drivers to the end of the IDE cables should not exceed 18". Therefore, the PIIX3 and buffers

should be located as close as possible to the IDE headers to allow the IDE cable to be as long as possible.

2.6.11 Clocks

- Refer to the 82430VX Layout Recommendations document for clock and general board layout recommendations.
- 3V CPU clocks—The CLK input on the P54 family is 5V tolerant. The CLK input on the P55C family is not 5V tolerant.
- USB Clock—48 MHz or 24 MHz with a duty cycle of better than 45/55% (24 MHz) or 40/60% (48 MHz) should be fed into the PIIX3's USB clock input, pin 146.
- Any one HCLK net must not have more than two loads associated with it. In general, (1) The Processor clock and the TVX clock should be on the same net. (2) Two separate HCLKs should be connected to any double sided DIMM. (3) Two separate HCLKs should be connected to the COAST module when supporting 512k of Pburst or 256K Pburst with 32Kx16 SRAM devices (when soldering down Pburst, do not exceed two loads per HCLK). And (4) If SDRAM is used in the system, a 74FCT163244 like device is required to provide the additional clocks (refer to the 82430VX reference schematics).

2.6.12 Flash

- 1-Mbit flash—1 Mbit of flash is generally all that is required to support the 82430VX, in all configurations (including SMBA). However, it is highly recommended that support for an optional 2M Boot Block Flash be designed in, even if a 1M device is planned (each size comes in a different package type). By simply laying out 2 pad sets, one for the 1M, and another for a 2M, the board will allow use of a 2M Flash, if the BIOS becomes too large for 1Mbit sometime in the near future.
- 2 Mbit or greater flash—If support for a 2-Mbit flash or greater is required, the BIOSCS# must be "OR'ed" with the XOE# signal and driven to the CE# input of the flash device. This is a 2M flash design consideration.

2.6.13 Layout

- Refer to the 82430VX Layout Recommendations document for clock and general board layout recommendations.
- Refer to the "82430FX PCIset IDE Layout Guidelines (Rev 1.x)" for IDE layout and general guidelines.

2.6.14 Miscellaneous

- It is highly recommended that the PWRGOOD signal from the power supply **not** be connected directly to logic on the board, without first going through a Schmitt trigger type circuitry to square-off and maintain the signal integrity or PWROK. Refer to the 82430VX reference schematics.

2.7 82430VX Reference Board Schematic Updates

(1) Schematic page 7: R41 should be changed to a resistor value of 4.7k–10k.

(2) Schematic page 13: The PIIX3 sysclk can be strapped for (divide by 4—60/66 MHz operation), and BIOS can then write bit 16, at PIIX3 register offset 68h, to set the divisor to 3 (50 MHz), if required. In this case, R68 and JP7 on schematic page 13 can be removed, and PWROK can then be tied directly to the 74F07 (U3C).

(3) Schematic page 13: Pin 134 TESTIN# should be pulled up to 5V using 4.7K to 20K resistor.

(4) Schematic page 14: Pin 28 on each IDE connector should be defined as an NC and tied high through 10k pull-ups. Pin 28 should not be connected to BALE.

(5) Schematic page 22,23: The IDSEL signal on each PCI connector should have a series resistor (~ 100 ohms) placed near each connector. This is a PCI recommendation.

(6) 330 ohm pull-up resistor onRefresh# should be changed to 1k pull-up.

3

Board Layout and Routing Guidelines

CHAPTER 3
BOARD LAYOUT AND ROUTING GUIDELINES

This section describes the Intel 430VX PCIset (430VX) layout and routing recommendations to insure a robust design. These guidelines should be followed as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

3.1 Placement

Examples of the recommended component placement for Pentium processor-based 430VX designs are shown below for a 2/3 baby AT form factor. The following two examples show a:

1. Shared Memory Buffer Architecture (SMBA) with EDO/FPM/SDRAM DRAM
2. EDO/FPM/SDRAM in a non-SMBA design

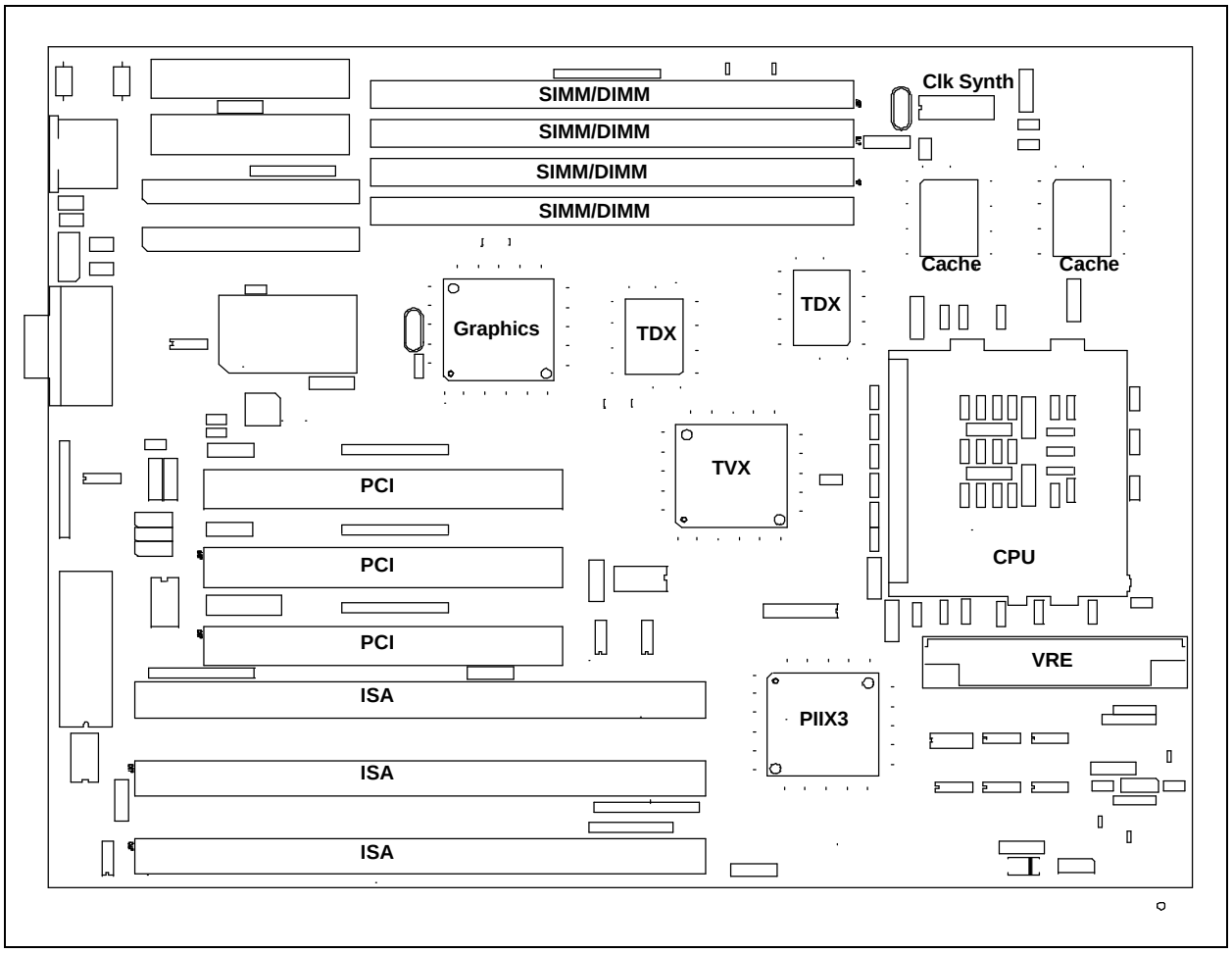


Figure 3-1. Example Placement for an SMBA and EDO/FPM/SDRAM DRAM 430VX Design

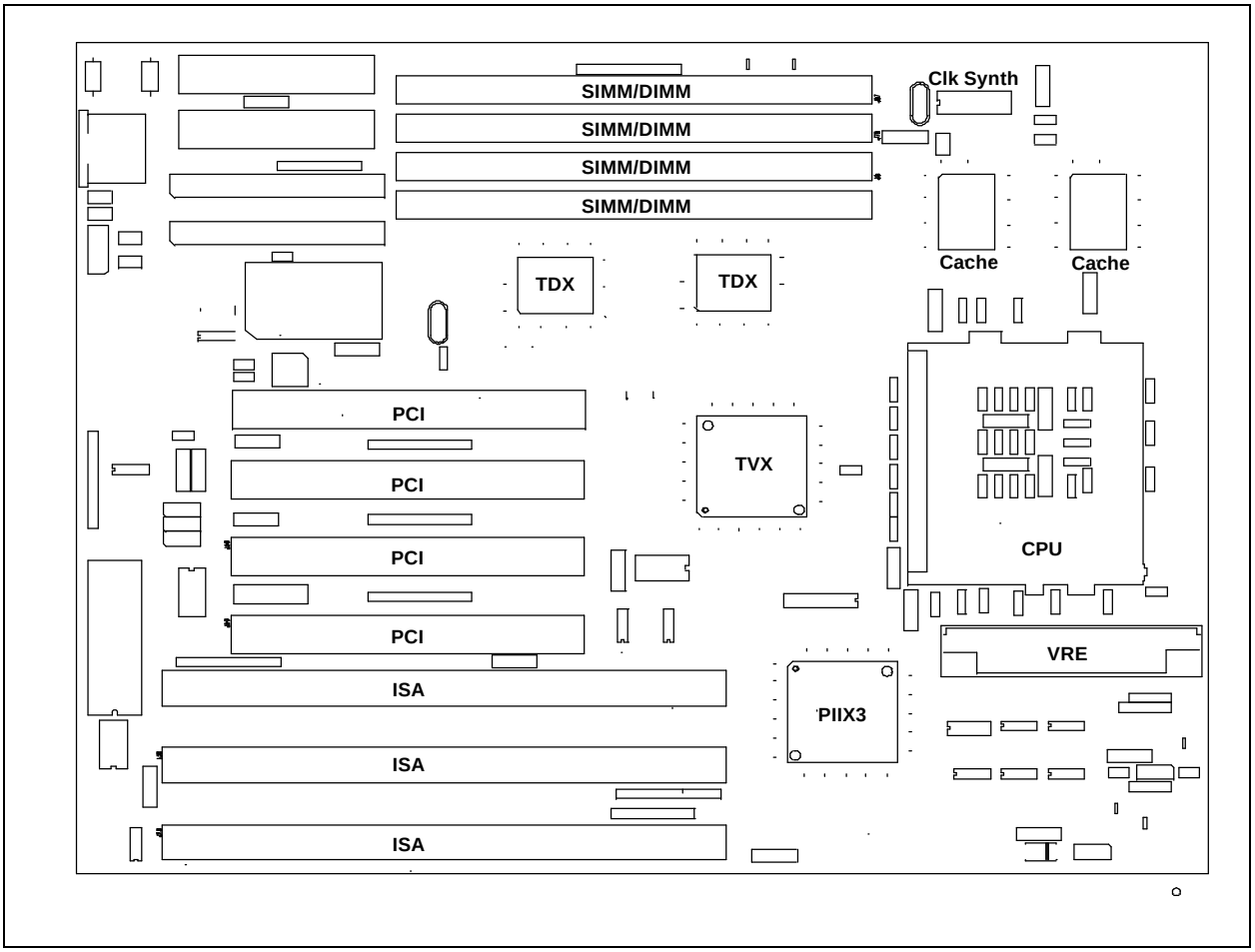


Figure 3-2. Example Placement for an EDO/FPM DRAM, SDRAM 430VX Design (non-SMBA)

3.2 Board Description

A 430VX motherboard can be designed using a 4 layer stack-up arrangement (Figure 3-3). The impedance of all the signal layers should be between 60 and 90 ohms. The overall board thickness is to be .062 inch.

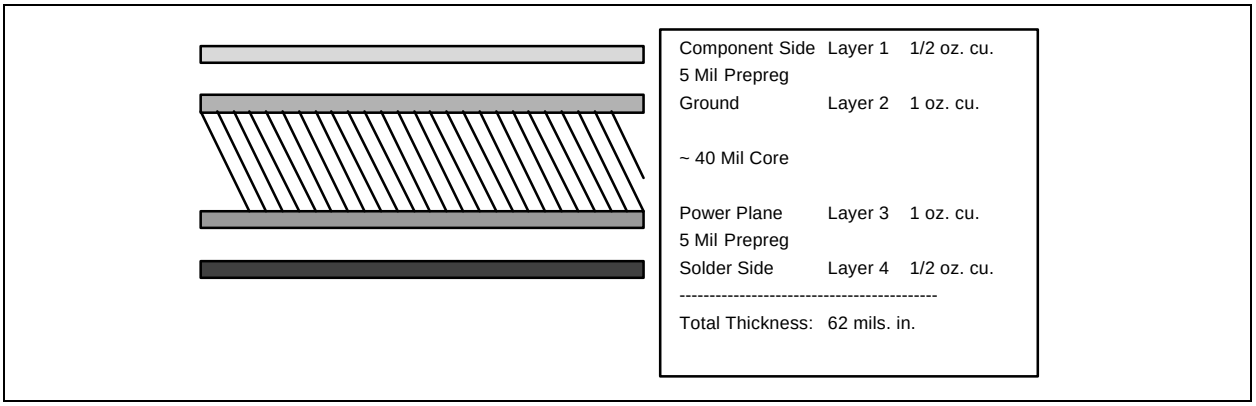


Figure 3-3. Four Layer Board Stack-up

Note that the top and bottom routing layers specify 1/2 oz. cu. However, by the time the board is plated, the traces will be about 1 to 1.5 oz. cu. Please check with your fabrication vendor on the exact value and insure that any signal simulation accounts for this.

Additional guidelines on board buildup, placement and layout include:

- The board impedance (Z) must be between 60 and 90 ohms (75 ohms ± 20%)
- FR-4 material should be used for the board fabrication
- The ground plane should not be split on the ground plane layer. If a signal must be routed for a short distance on a power plane, then it should be routed on the V_{CC} plane, not the ground plane
- Group 5V and 3V components near each other. This allows for fewer isolated V_{CC} islands on the power plane

3.3 Layout and Routing Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order of which signals are routed first and last will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high speed bus signals first. Either order can be used, as long as the guidelines listed here are followed.

3.3.1 General Guidelines

It is recommended that the address, data, and control signals are routed using a “daisy chain” topology. The use of this topology implies that no stubs are to be used to connect any devices on the net. Figure 3-4 shows two possible techniques to achieve a stubless trace.

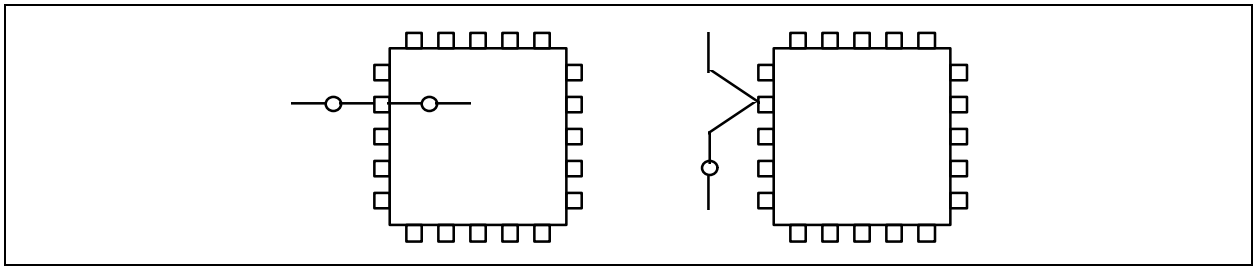


Figure 3-4. Stubless Routing Examples

In instances where it is not possible to apply one of these two techniques (e.g., due to congestion), a very short stub is allowed. Figure 3-5 shows a trace with a short stub connecting the pin.

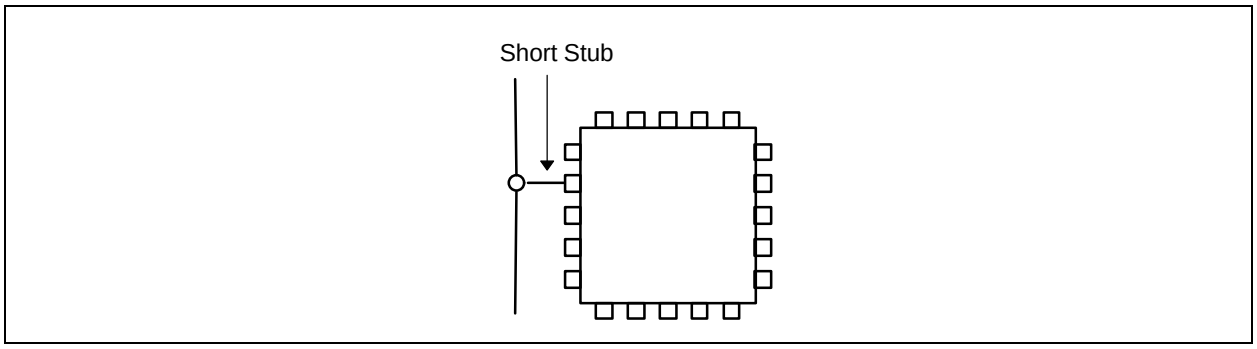


Figure 3-5. Short Stub Routing Example

3.3.2 Memory/Cache Layout Guidelines

The 430VX supports a range of design options. The key options that must be determined before layout and routing are:

1. The number of rows of memory will the design support
2. Type of DRAM module used (DRAM, SDRAM, or both)
3. Whether SMBA (Shared Memory Buffer Architecture) will be used
4. Type of cache supported (PBS vs. Asynch, 256 KB vs. 512 KB)

The possible DRAM and system options supported by the 430VX are shown in Table 3-1.

Table 3-1. Memory/Cache Types Supported by 430VX

Memory Component	Description
DRAM Type:	FPM, EDO, SDRAM
DRAM/SDRAM Module Type:	72-pin SIMM: 32 bit, 168-pin DIMM: 64 bit
DRAM/SDRAM Voltage:	3.3V, 5.0V
Number Of Rows Of Memory:	1 to 5
DRAM Speed:	50, 60, 70 ns
DRAM Component Width:	x4, x8, x16
SDRAM Speed:	66/60/50 MHz, RAS-to-CAS latency=3 clocks
SDRAM Component Width:	x8, x16
Cache Type:	Pipelined Burst SRAM, Asynchronous
Cache Size:	256K, 512K
CPU Bus Frequency:	50, 60, 66 MHz

In the following description the term ‘row’ or ‘row of memory’ describes 64 bits of memory connected to the same RAS# signal. There are a few different ways to create a row of memory that include the following:

- 2 single density 72-pin SIMMs = 1 row (1 RAS# line) of memory
- 2 double density 72-pin SIMMs = 2 rows (2 RAS# lines) of memory
- 1 single density 168-pin DIMM = 1 row (1 RAS# line) of memory
- 1 double density 168-pin DIMM = 2 rows (2 RAS# lines) of memory
- A fifth row is available that supports 1Mx16 and 2Mx8 devices. This 5th RAS line is intended for soldered down memory. Note that if the 5th RAS line is used, all RAS lines must use the same type of memory as the 5th RAS line (i.e. EDO/FPM vs. SDRAM). If an SMBA graphics controller is used, the 5th RAS line is restricted to 8 MB of memory.

For the above options, the following layout guidelines are provided for four system implementation options.

1. 1 to 5 rows of memory using DRAM SIMM modules with SMBA. The 5th row is soldered down
2. 2 rows of DRAM SIMMs with 2 rows of an SDRAM DIMM with SMBA
3. 1 to 5 rows of memory using SDRAM DIMMs in a non-SMBA design
4. 256-KB/512-KB Pipelined Burst SRAM and 256-KB/512-KB asynchronous cache

The tables below show the recommended maximum trace lengths for each of the 430VX high speed interfaces. The maximum trace lengths are divided into the following tables.

- Host/Cache interface for PBurst SRAM (256K/512K)
- Host/Cache interface for Asynch SRAM (256K/512K)
- Table 3-4 TVX/TDX interface
- Table 3-5 EDO/FPM DRAM interface with SMBA (5 RAS lines)
- Table 3-6 EDO/FPM DRAM and SDRAM interface with SMBA (2 RAS lines for the SIMMs and 2 RAS lines for the DIMM)
- SDRAM interface only (non-SMBA)

These guidelines should be followed as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

Table 3-2. Host/Cache Interface Guidelines for a Pipelined Burst SRAM Cache Design

Signals	Driver	Receiver(s)	Max Length (point-to-point)	Comments
HA(18:3)	CPU	SRAM	5.5”	Note 1
HA(18:3)	CPU	Tag	4.0”	Note 1
HA(18:3)	TVX	SRAM	6.5”	Note 1
HA(31:3)	CPU	TVX	6.0”	Note 1
HA(31:3)	TVX	Tag	4.0”	Note 1
BE(7:0)#	CPU	TVX	5.5”	Note 1
BE(7:0)#	CPU	SRAM	8.0”	Note 1
HD(63:0)	CPU	TDX	4.5”	Note 2
HD(63:0)	TDX	SRAM	4.5”	Note 2
HD(63:0)	CPU	SRAM	3.5”	Note 2
BRDY#, BOFF#, NA#, KEN#/INV, AHOLD, EADS#, CACHE#	TVX	CPU	5.0”	
ADS#, MIO#, D/C#, HLOCK#, W/R#, HITM#, SMIACT#	CPU	TVX	5.0”	
CADV#, CADS#	TVX	SRAM	6.0”	
CCS#	TVX	SRAM	6.0”	
COE#	TVX	SRAM	6.0”	
GWE#	TVX	SRAM	6.0”	
BWE#	TVX	SRAM	6.0”	
TIO(7:0)	TVX	Tag	6.0”	
TWE#	TVX	Tag	6.0”	

NOTES:

1. Keep the total cumulative Host Address length less than 12”.
2. Keep the total cumulative Host Data Bus less than 6.5”.

Table 3-3. Host/Cache Interface Guidelines for an Asynchronous Cache Design

Signals	Driver	Receiver(s)	Max Length (point-to-point)	Comments
HA(18:3)	CPU	Buffer	5.0”	Note 1
HA(18:3)	CPU	Tag	5.0”	Note 1
HA(18:3)	Buffer	Asynch Cache	4.0”	Note 1
HA(18:3)	TVX	Tag	4.0”	Note 1
HA(31:3)	CPU	TVX	7.0”	Note 1
BE(7:0)#	CPU	TVX	5.5”	Note 1
BE(7:0)#	CPU	SRAM	8.0”	Note 1
HD(63:0)	CPU	TDX	4.5”	Note 2
HD(63:0)	CPU	SRAM	3.5”	Note 2
BRDY#, BOFF#, NA#, KEN#/INV, AHOLD, EADS#, CACHE#	TVX	CPU	5.0”	
ADS#, MIO#, D/C#, HLOCK#, W/R#, HITM#, SMIACT#	CPU	TVX	5.0”	
CAA/CAB(4:3)	TVX	Asynch SRAM	6.0”	
COE#	TVX	Asynch SRAM	6.0”	
CGCS#	TVX	Asynch SRAM	6.0”	
BWE#	TVX	Asynch SRAM	6.0”	
TIO(7:0)	TVX	Tag	6.0”	
TWE#	TVX	Tag	6.0”	

NOTES:

1. Keep the total cumulative Host Address length less than 12”.
2. Keep the total cumulative Host Data Bus less than 6.5”.

Table 3-4. TVX and TDX Interface Guidelines

Signals	Driver	Receiver(s)	Max Length (point-to-point)	Comments
PLINK(15:0)	TVX/TDX	TVX/TDX	3.0”	
MSTB(1:0)	TVX	TDX	3.0”	
MADV#	TVX	TDX	3.0”	
PCMD(1:0)	TVX	TDX	3.0”	
MXS	TVX	TDX	3.0”	
HOE#	TVX	TDX	3.0”	
MOE#	TVX	TDX	3.0”	
POE#	TVX	TDX	3.0”	

Table 3-5. Memory Interface Guidelines for an SMBA and EDO/FPM Design with 1 to 5 Rows

Signals	Driver	Receiver(s)	Max Length (point-to-point)	Comments
RAS(3:0)#	TVX	DRAM	8”	Note 1
CAS(7:0)#	TVX	DRAM	8”	Note 1
MA(11:0)	TVX	DRAM	8”	Note 1
WE(B:A)#	TVX	DRAM	6”	Note 1
MD(63:0)	TDX	DRAM	6”	Note 1
RAS(3:0)#	Graphics	DRAM	8”	Notes 1, 2
CAS(7:0)#	Graphics	DRAM	8”	Notes 1, 2
MA(11:0)	Graphics	DRAM	8”	Notes 1, 2
WE(B:A)#	Graphics	DRAM	6”	Notes 1, 2
MD(63:0)	Graphics	DRAM	6”	Notes 1, 2

NOTES:

1. Keep the total cumulative trace length less than 12”.
2. The graphics controller drive strength is assumed to be similar to the 430VX drive strength. Please contact the graphics controller vendor for more information.

Table 3-6. Memory Interface Guidelines for an SMBA and EDO/FPM/SDRAM Design with 1 to 4 Rows

Signals	Driver(s)	Receiver(s)	Max Length (point-to-point)	Comments
CS(3:0)#	TVX or Graphics	SDRAM	6”	Notes 1, 2
DQM(7:0)	TVX or Graphics	SDRAM	6”	Notes 1, 2
SRAS(B:A)#	TVX or Graphics	SDRAM	6”	Notes 1, 2
SCAS(B:A)#	TVX or Graphics	SDRAM	6”	Notes 1, 2
MA(11:0)	TVX or Graphics	SDRAM	8”	Notes 1, 3
WE(B:A)#	TVX or Graphics	SDRAM	6”	Notes 1, 2
RAS(3:0)#	TVX or Graphics	DRAM	8”	Notes 1, 2
CAS(7:0)#	TVX or Graphics	DRAM	8”	Notes 1, 2
MA(11:0)	TVX or Graphics	DRAM	8”	Notes 1, 3
WE(B:A)#	TVX or Graphics	DRAM	6”	Notes 1, 2
MD(63:0)	TDX or Graphics	DRAM/SDRAM	6”	Notes 1, 2

NOTES:

1. Keep the total cumulative trace length less than 9”.
2. The graphics controller drive strength is assumed to be similar to the 430VX drive strength. Please contact the graphics controller vendor for more information.
3. Keep the total cumulative trace length less than 12”.

Table 3-7. Memory Interface Guidelines for an SDRAM only Design with 1 to 5 Rows

Signals	Driver	Receiver(s)	Max Length (point-to-point)	Comments
CS(3:0)#	TVX	SDRAM	6”	Note 1
DQM(7:0)	TVX	SDRAM	6”	Note 1
SRAS(B:A)#	TVX	SDRAM	6”	Note 1
SCAS(B:A)#	TVX	SDRAM	6”	Note 1
MA(11:0)	TVX	SDRAM	8”	Note 1
MD(63:0)	TDX	SDRAM	6”	Note 1
WE(B:A)#	TVX	SDRAM	6”	Note 1

NOTES:

1. Keep the total cumulative trace length less than 9”.

3.3.3 Memory/Cache Routing Guidelines

Figure 3-6 and Figure 3-7 show the recommended component placement and routing. Figure 3-6 shows routing for the host address and memory address lines with an SMBA graphics controller. This memory data line routing applies both to SIMM and DIMM implementations. The TVX-to-TDX interconnect routing is also shown.

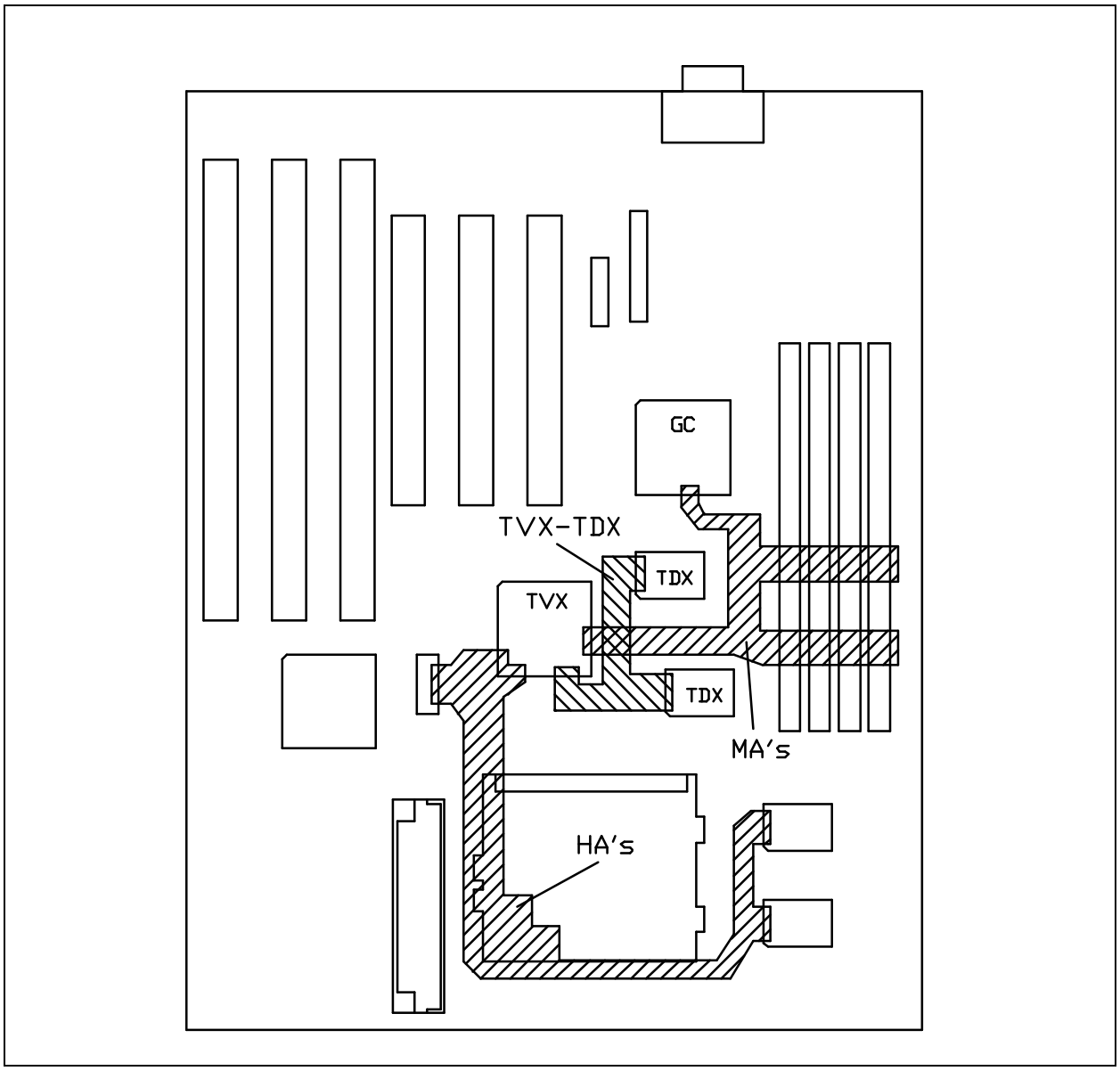


Figure 3-6. 430VX Routing Example of HA, MA Lines, and the TVX/TDX Interface (SMBA)

Figure 3-7 shows the host data and memory data bus routing for an SMBA design. This memory data bus routing applies both to DIMM and SIMM implementations.

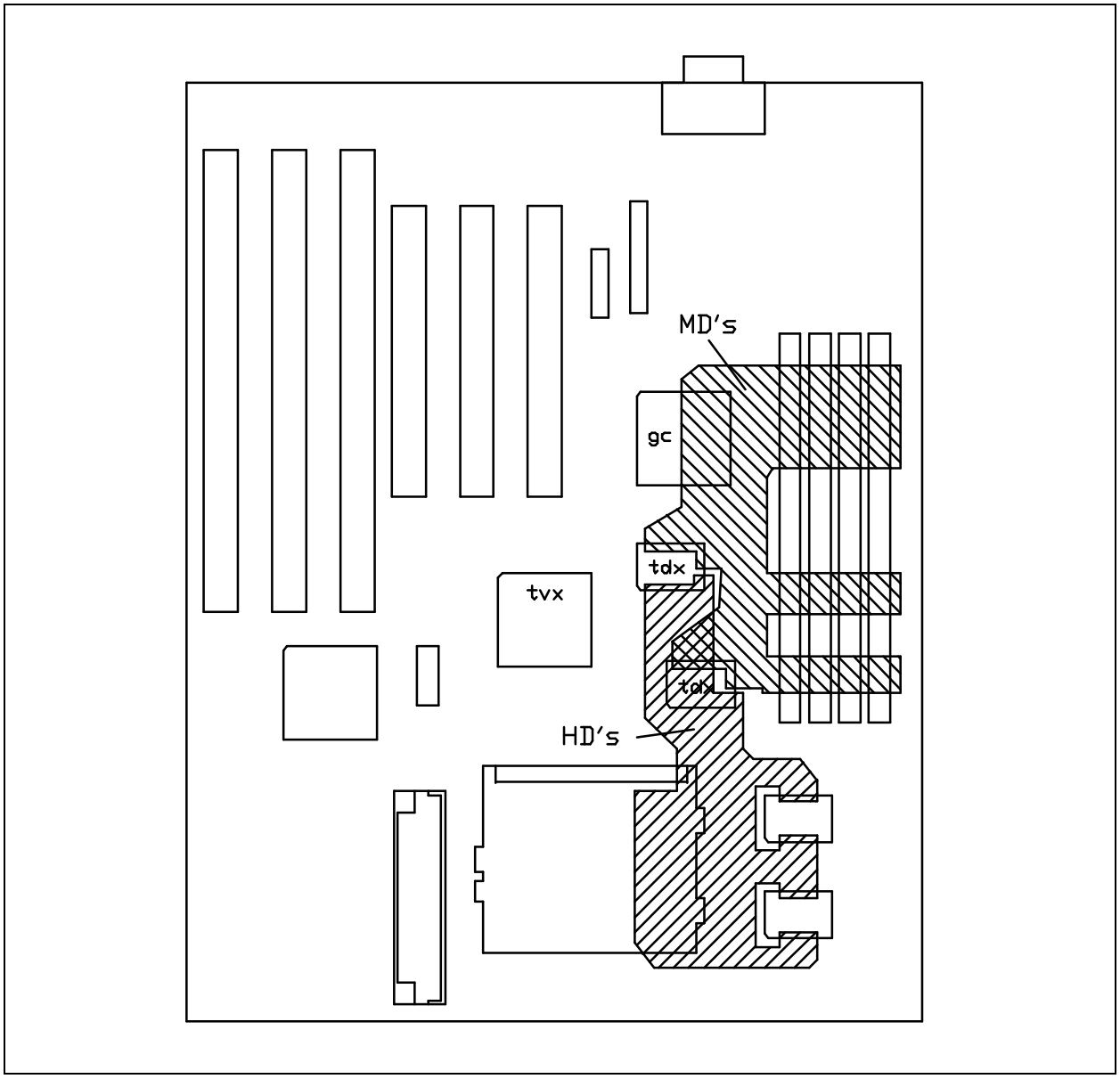


Figure 3-7. 430VX Routing Example of the MD and HD Lines (SMBA)

Figure 3-8 shows routing for the host address and memory address lines for a non-SMBA design. This memory data line routing applies both to SIMM and DIMM implementations. The TVX and TDX interconnect routing is also shown.

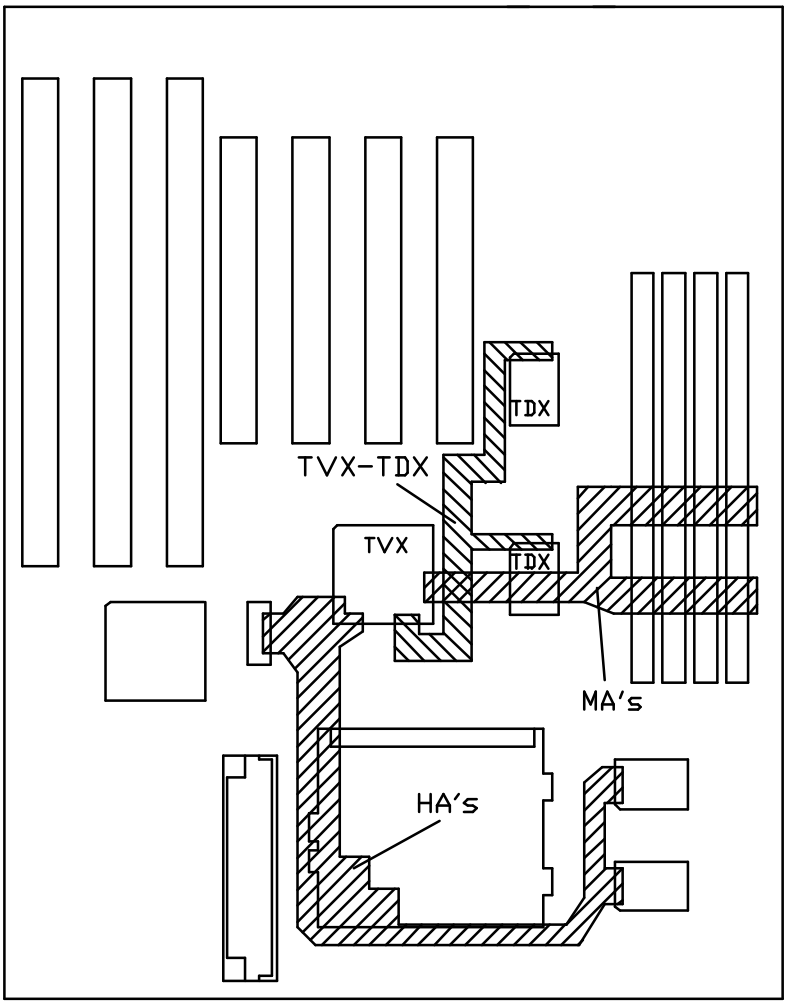


Figure 3-8. 430VX Routing Example of HA, MA lines, and the TVX/TDX Interface (non-SMBA)

Figure 3-9 shows the host data and memory data bus routing for a non-SMBA design. This memory data bus routing applies both to DIMM and SIMM implementations.

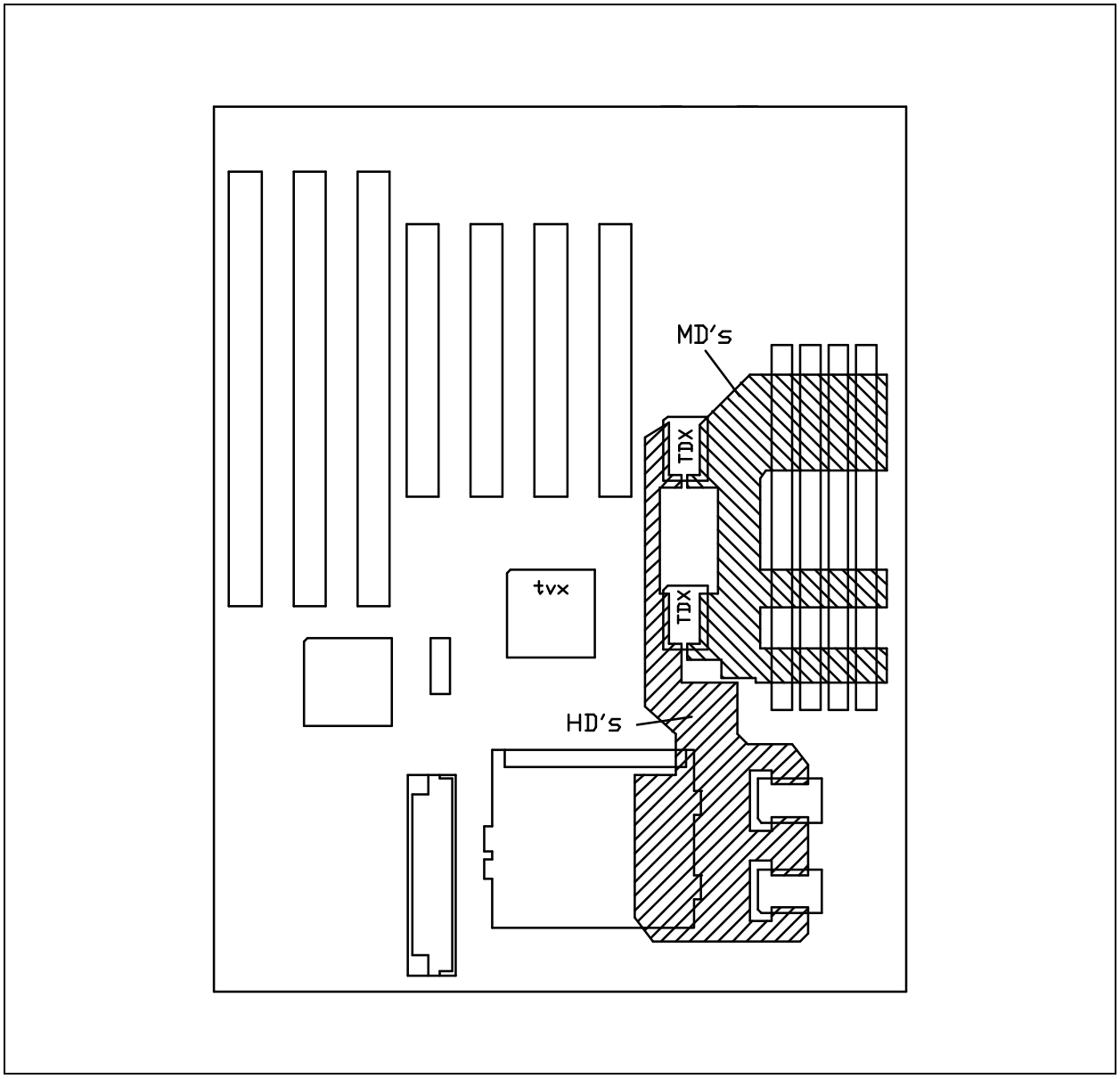


Figure 3-9. 430VX Routing Example of the MD and HD Lines (non-SMBA)

3.3.4 Clock Routing Guidelines

Table 3-8 summarizes the clocking requirements in a 430VX system design.

Table 3-8. Clocks in a 430VX System

Host Clocks	PCI Clocks	Miscellaneous
Pentium® processor	TVX	USB (24 or 48 MHz)
TVX	PIIX3	Keyboard (12 MHz)
TDX	3-4 PCI Slots	Floppy clock (24 MHz)
SDRAM (2 clocks per DIMM socket)	SMBA graphics controller if implemented	ISA bus OSC (14 MHz)
SMBA graphics controller if implemented		Bus Clock (8 MHz from PIIX3)
SRAM (1 clock per 2 loads)		

The host and PCI clock routing require the most attention to detail. Complete clock generation specifications are listed in the 430VX System Clock Requirements section of this document. Below are some additional host and PCI clock routing guidelines.

3.3.4.1 Host Clock Skew Requirements

The total skew between any two host clock loads must be less than +1.0 ns, with the exception of the Pentium processor to the TVX which must be +0.3 ns. The clock synthesizer must guarantee a maximum skew of 250 ps between any two host clock outputs. The system design must guarantee a maximum flight time skew of 750 ps between any two host clock receivers.

If SDRAM is implemented, then a 74FCT163244 buffer must be used to create more copies of the host clock since each SDRAM DIMM requires four host clocks. One output of the clock synthesizer is tied to multiple inputs of the 74FCT163244 buffer. The 74FCT163244 buffer then provides all the host clocks to the system. The 74FCT163244 buffer provides a pin-to-pin jitter of +500 ps (please refer to the Third Party Vendor List document).

Extreme care should be taken when routing the SDRAM host clocks in order that a +1.5 ns maximum skew is maintained with respect to the other host clocks. The DIMMs can place 2 loads/per host clock (x16 single density) up to 8 loads/per host clock (x8 double density), x4 devices are not recommended due to the excessive loading. The SDRAM clock layout needs to take these above factors into consideration to maintain proper signal integrity and clock skew requirements.

If an SMBA graphics controller is used and SDRAM is not used, the clock synthesizer component should have five host clock outputs. In this way a 74FCT163244 buffer will not be required to create an extra copy of the host clock for the graphics controller, only a clock synthesizer will be required (please refer to the Third Party Vendor section for a parts list).

3.3.4.2 Host Clock to PCI Clock

The clock synthesizer must guarantee a delay from the host clock output to the PCI clock outputs. The minimum delay must be 1 ns and the maximum delay should not exceed 5 ns. The system must insure that the host clock to PCI clock skew at the TVX is a minimum of +1 ns and a maximum of +7 ns. This means that all of the PCI clock flight times should be guaranteed to be the same or longer than the host clock flight times. If SDRAM is implemented then a 74FCT163244 buffer must also be used for the PCI clocks. The PCI clocks and host clocks must both come from the 74FCT163244 buffer in order to maintain the host-to-PCI clock skew relationship (+1n to +7 ns at the input of the TVX).

3.3.4.3 PCI Clock Skew

The total skew between any two PCI clock loads must be less than 2.0 ns. The clock synthesizer must guarantee a maximum skew of 500 ps between any two PCI clock outputs. The system design must guarantee a maximum flight time skew of 1.5 ns between any two PCI clock receivers. PCI clock traces to on-board components should be 2.5 inches longer than PCI clock traces going to PCI slots to help minimize skew.

The maximum length on any of the PCI clocks to motherboard devices should be less than 15 inches and should be less than 12.5 inches to any PCI add-in slot. Any clock signals crossing from 3.3V area to 5V should cross the boundary adjacent to the ground plane.

3.3.5 Host Clock Layout for an EDO/FPM, SDRAM, and SMBA Design

Following are the layout recommendations for the host clock, and PCI clock signals being driven from the clock chip. The requirement is to drive up to twenty five HCLK loads from eight pins, and seven PCICLK loads from seven pins with the following rising edge maximum skews.

Table 3-9. Rising Edge Maximum Skews

Clock Relationship	Skew Requirements	Comments
Host clock	±1.0 ns	Measured at 1.5V rising edge at the inputs
PCI clock	±2.0 ns	Measured at 1.5V rising edge at the inputs
CPU clock to TVX clock	±0.3 ns	Measured at 1.5V rising edge at the inputs
TVX Host clock to TVX PCI clock	+1.0 ns to +7.0 ns	Measured at 1.5V rising edge at the TVX inputs
SDRAM Host clocks to other Host clocks	±1.5 ns	Measured at 1.5V rising edge at the SDRAM inputs
74FCT163244 output pin-to-pin skew	500 ps	Measured at 1.5V rising edge at the output buffer

Where: D < 1.0”

C + D = 3.0”

Note that trace length ‘A’ is primarily dictated by the host clock-to-CPU trace.

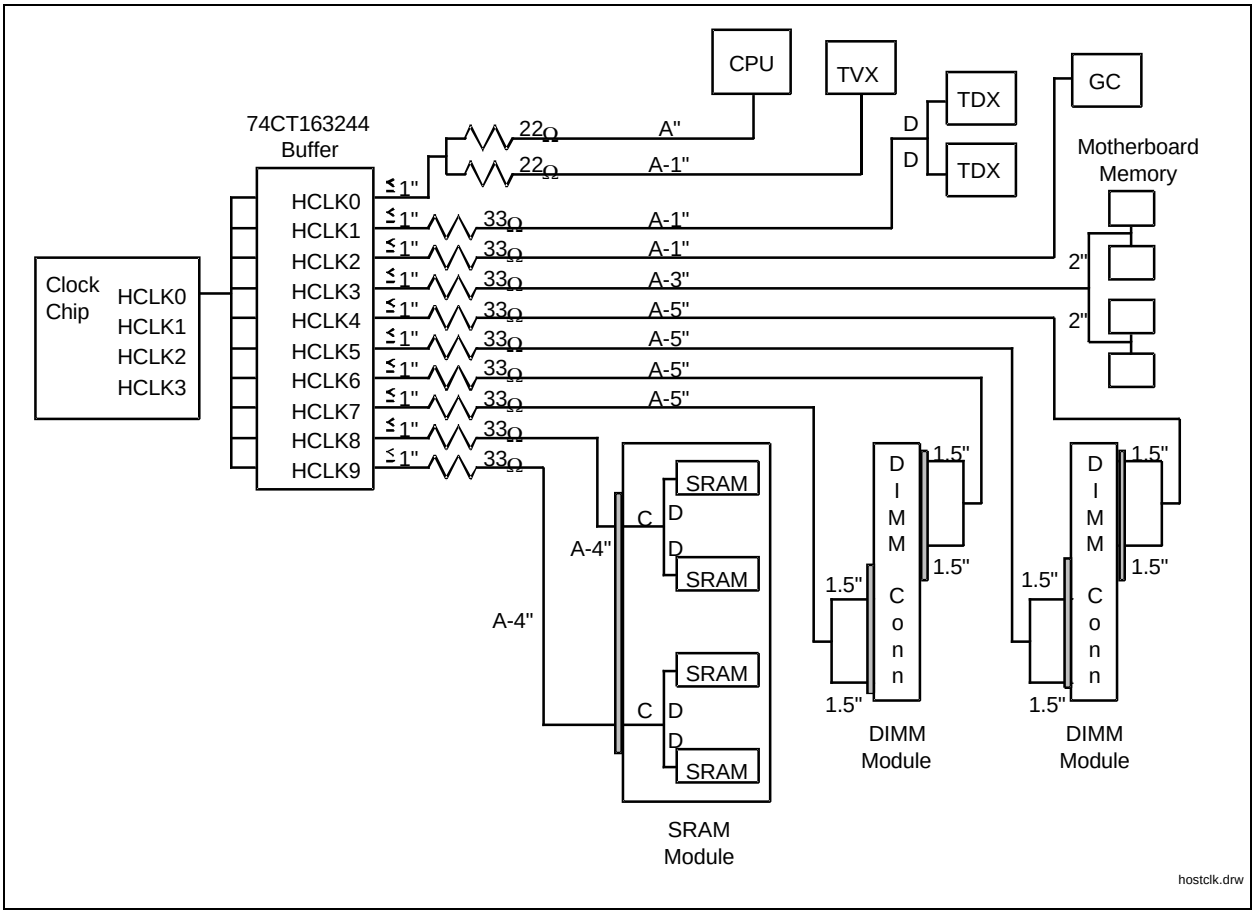


Figure 3-10. Host Clock Layout Recommendation for an SDRAM/SMBA Design

3.3.6 PCI Clock Layout for an SDRAM/SMBA Design

Figure 3-11 shows the PCI clock layout recommendation using a 74FCT163244 buffer. This buffer is only required if implementing SDRAM in the system. Both the host clocks and PCI clocks must come from the buffer if using a buffer to create copies of the host clock.

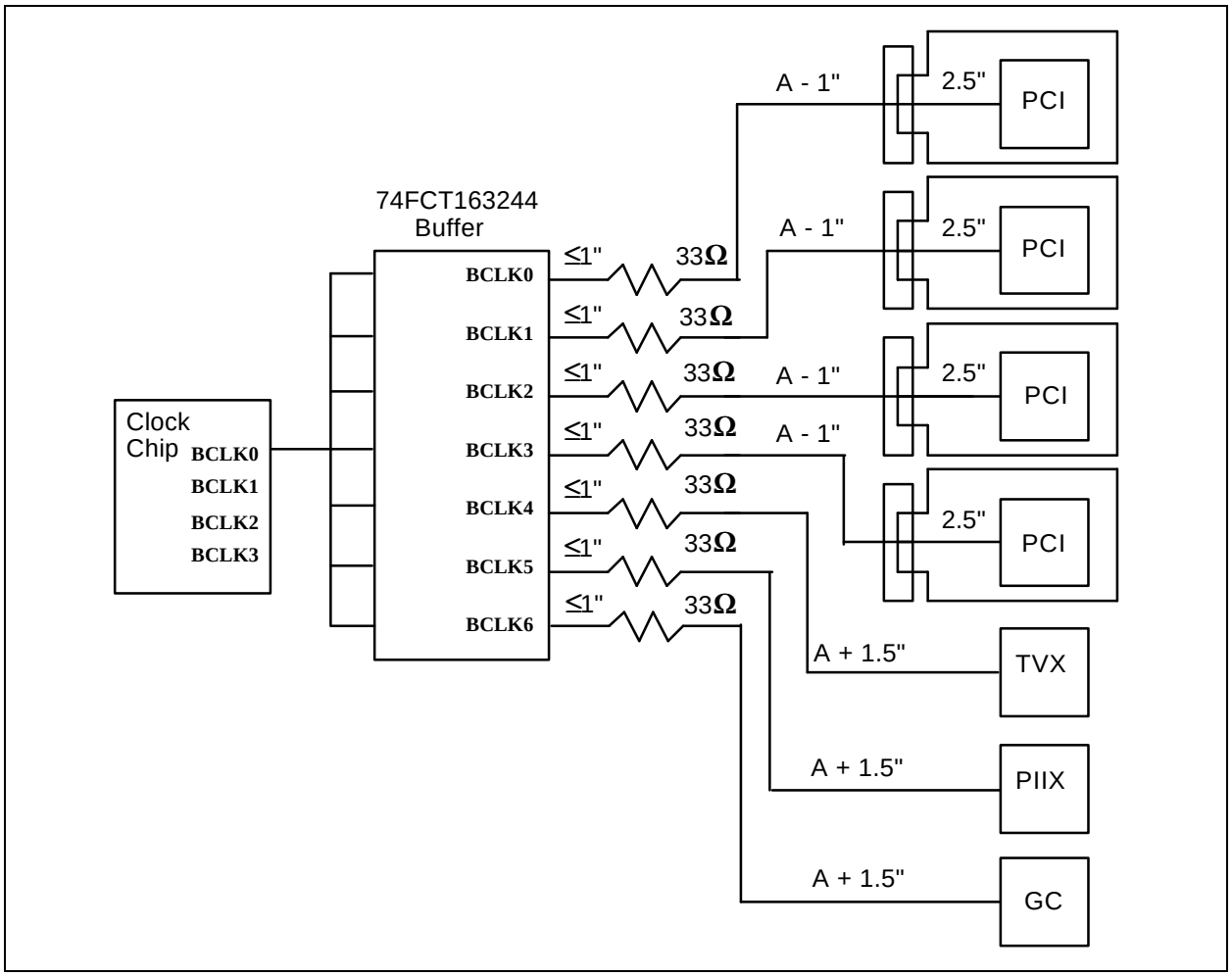


Figure 3-11. PCI Clock Layout Recommendation for an SDRAM/SMBA Design

3.3.7 Host Clock Layout for an EDO/FPM Only System with SMBA

Following is the host clock layout for an EDO/FPM only system with SMBA. Note that the clock synthesizer component has five host clock outputs. If an SMBA graphics controller is not used, a clock synthesizer component with only four host clock outputs can be used.

Host clock layout requirement where:

D < 1.0”
C + D = 3.0”

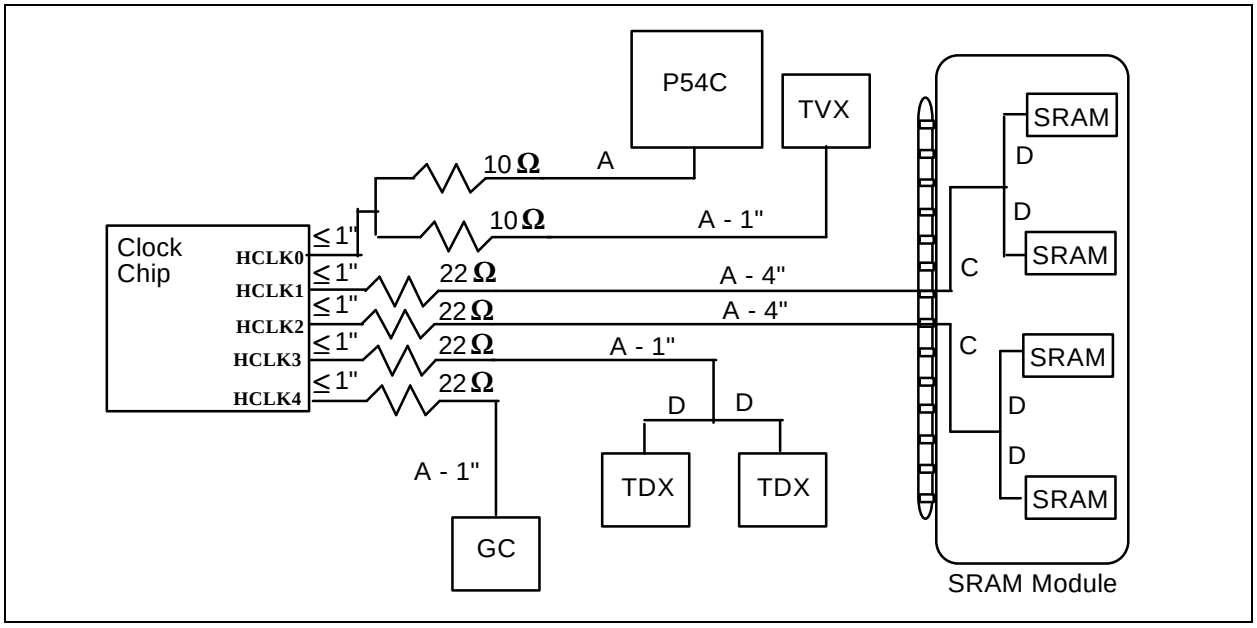


Figure 3-12. Host Clock Layout for an EDO/FPM System with SMBA

3.3.8 PCI Clock Layout for an EDO/FPM Only System with SMBA

Figure 3-13 shows the PCI clock layout recommendation for an EDO/FPM system with an SMBA graphics controller. Note that there can be only 3 PCI slots when using an SMBA graphics controller.

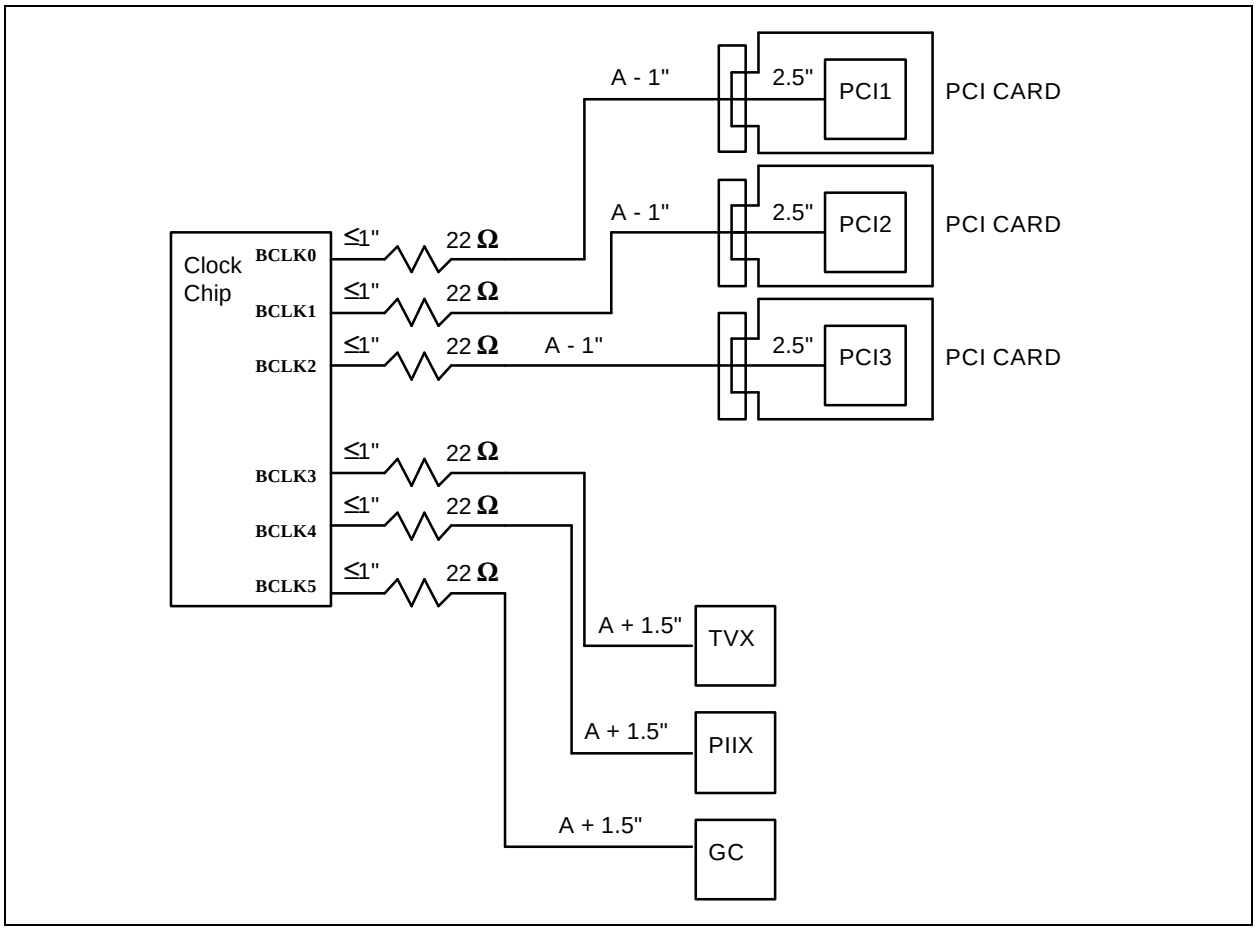


Figure 3-13. PCI Clock Layout for an EDO/FPM and SMBA System

3.3.9 IDE Routing Guidelines

This section contains guidelines for connecting and routing the PIIX3 IDE interface. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination. The current recommendations use 47 ohm resistors on DIOR#/DIOW#, while the remaining signals use resistors between 22 and 47 ohm resistors.

Cabling

1. **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
2. **Capacitance:** Less than 30 pF.
3. **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
4. **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

Motherboard

1. **PIIX3 Placement:** The PIIX3 should be placed as close as possible to the ATA connector(s).

2. **Resistor Location:** When the distance between the PIIX3 and the ATA connectors exceeds 4 inches the series termination resistors should be placed within 1 inch of the PIIX3. Designs that place the PIIX3 within 4 inches of the ATA connectors can place the series resistors anywhere along the trace. Figure 3-14 shows
   a placement example.
3. **Capacitance:** The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
4. **Series Termination:** The following resistor values are the current recommendations.

Signal	Resistor	Signal	Resistor
DD[15:0]	22–47Ω	CS1P#	22–47Ω
DA[2:0]	22–47Ω	CS1S#	22–47Ω
DIOR#	47Ω	CS3P#	220–47Ω
DIOW#	47Ω	CS3S#	22–47Ω
DDRQ0	22–47Ω	DIRQ1	22–47Ω
DDRQ1	22–47Ω	DDAK0	22–47Ω
DIRQ0	22–47Ω	DDAK1	22–47Ω
RESET*	22–47Ω		

*RESET comes from the PIIX3 RSTDRV signal through a schmitt trigger

One resistor per IDE connector is recommended for all signals. For signals labeled as 22 ohms–47 ohms, the correct value should be determined for each unique motherboard design, based on signal quality.

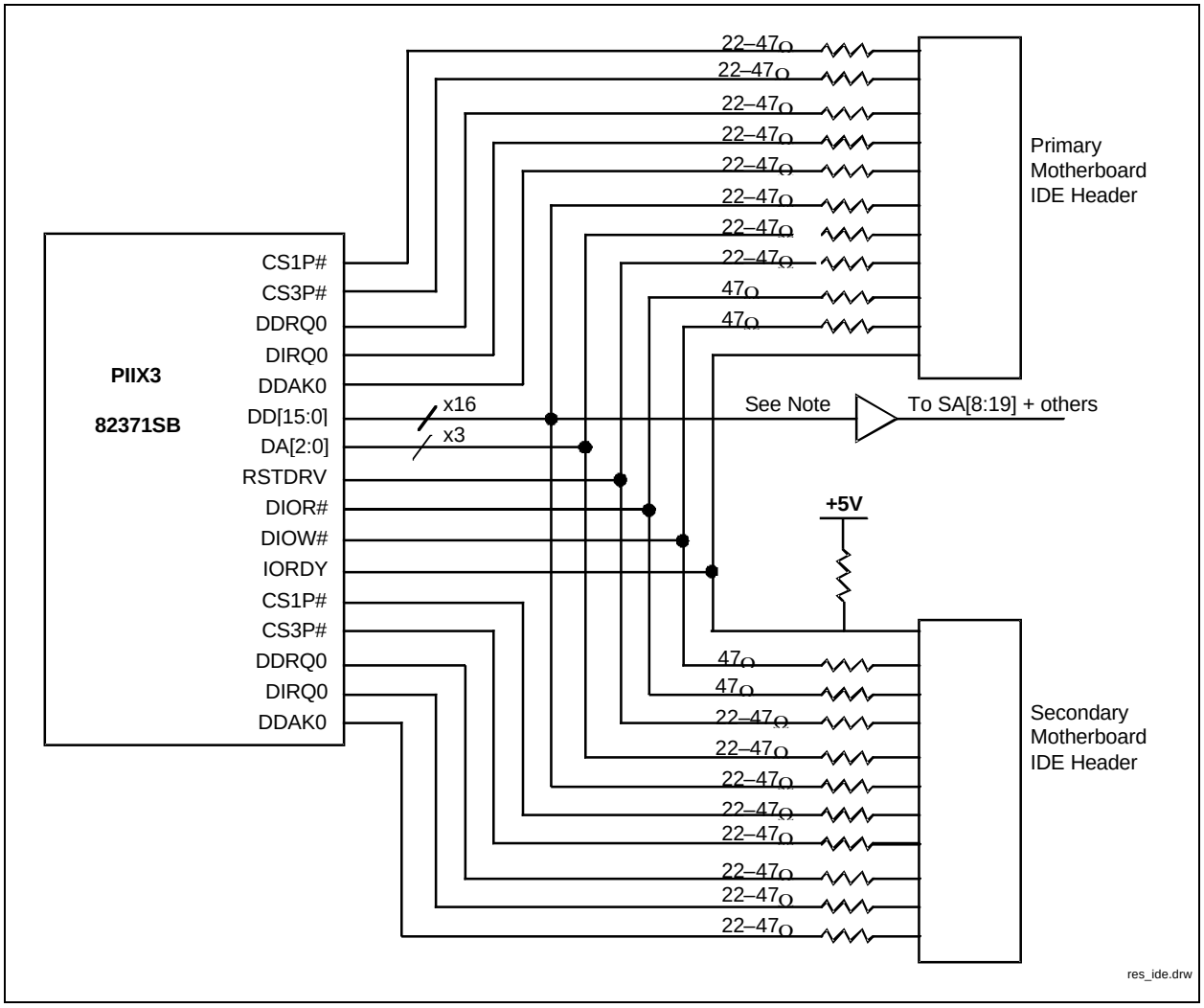


Figure 3-14. Series Resistor Placement for IDE Connectors

The design consideration shown in Figure 3-14 illustrates the series resistor placement for trace lengths not exceeding 4 inches. Note that if the trace length between the PIIX3 and the IDE header exceeds 4 inches, the series resistors should be placed within 1 inch of the PIIX3. The series termination resistors are required in either design.

For signals that go to both connectors, the length on each side of the T (where the trace splits to go to each resistor then connector) should be as small as possible (shown above).

Note that the DD[15:0] are buffered to generate the SA[19:8], SBHE# and APICCS# signals. If possible, route the DD[15:0] traces from the PIIX3 to the buffer input pins, then to the split for the two resistors as shown below. Otherwise, keep any additional stub length from the PIIX3 DD[15:0] trace to the buffer input as short as possible.

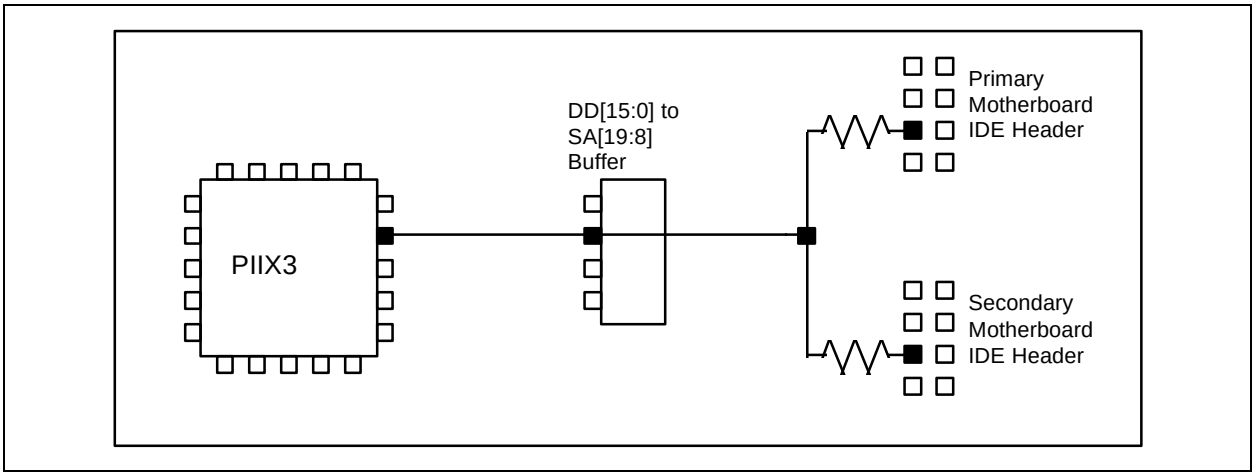


Figure 3-15. Layout Guideline for DD[15:0]

3.3.10 USB Power Distribution Layout Guideline

Following are general guidelines for USB power line and ground line:

- Each V_{CC} power line should be bypassed with no less than a 120 µf tantalum capacitor for each USB port. It should be placed between ferrite bead and EMI bypass capacitor on V_{CC}. The bypass capacitors should have a low dissipation factor to allow decoupling at higher frequencies.
- Ferrite beads and bypass caps are recommended on V_{CC} and V_{SS}, the USB power and ground lines, to minimize EMI radiation. They should be placed as close as possible to the USB connector. The capacitor values should be between 0.01 µf and 0.10 µf. The recommended value of ferrite beads is 100 ohms at 100 MHz.
- PolySwitch fuses, standard fuses, or some type of solid state switch should be used on each power line for overcurrent protection. USB spec requires that current be limited to 5 units load (1 unit = 100mA) for each USB port. However, the circuit protector must be chosen so that it will not trip for power on or dynamic attach transient current. The reasonable value for the trip current is 1.5A to 2.0A, and it shall not exceed 5A maximum.

Table 3-10. DC Electrical Characteristics on V_{CC}

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (Powered Host)	V_{CC}	4.75	5.25	V	1
Supply Current (Powered Host)		500		mA	2, 3

NOTES:

1. The minimum supply voltage is 4.75V on USB port after voltage drop on power line and connector. A minimum of 120 µf tantalum cap is needed for a maximum 330 mV droop.
2. The supply current cannot exceed 5.0A. The recommended trip current (minimum) is 1.5A–2.0A.
3. The recommended time not to trip is 100 µs minimum for solid state switch circuit for power on and dynamic attach transient current.

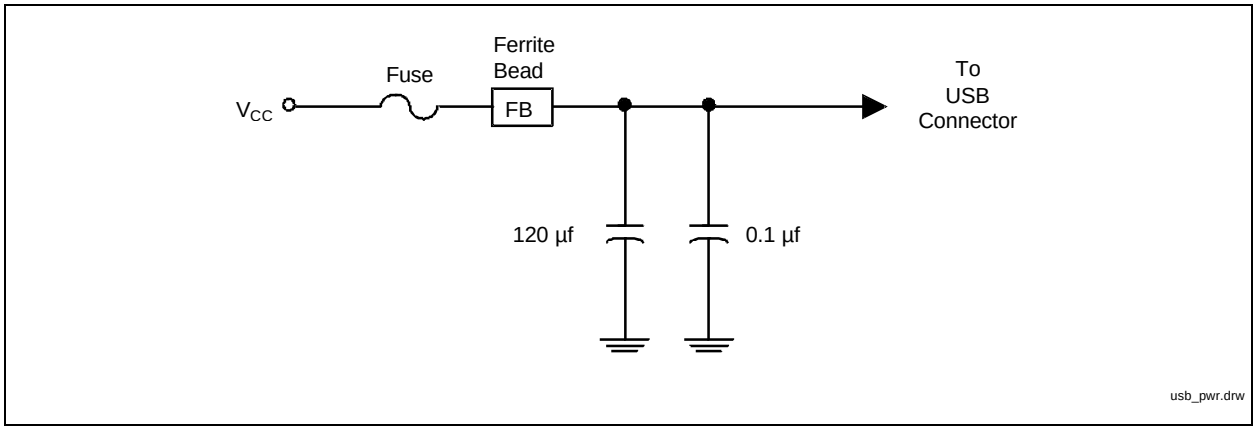


Figure 3-16. USB Power Distribution Layout

3.3.11 USB Motherboard Layout Guidelines for USB Data Signals

Please refer to the "PIIX3 USB Design Guide and Checklist" to obtain updated layout recommendations.

The goal of the following routing guidelines are to minimize the effects of ringing, crosstalk, and EMI radiation in the USB data signal lines. It is very important to ensure that high frequency system signals do not couple to the USB signals and radiate out on the USB cable. This is done by carefully matching the motherboard circuitry impedance to that of the twisted pair USB cable, by controlling signal rise and fall times, and by careful routing of the USB signals on the motherboard.

Following are general guidelines for the USB interface:

- 27 ohm series resistors should be placed as close as possible to the PIIX3 (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pF caps must be placed as close to the PIIX3 as possible and on the PIIX3 side of the series resistors on the USB data lines (P0±, P1±). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kohm ±5% pulldown resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±), and are REQUIRED for signal termination by USB specification. The length of stub should be as short as possible.
- The trace impedance for the P0±, P1± signals should be 45 ohms (to the ground) for each USB signal P+ or P-. The impedance is 90 ohms between the differential signal pairs P+ and P- to match the 90 ohm USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 ohms is the series impedance of both wires, resulting in an individual wire presenting a 45 ohms impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as 'critical signals' (i.e., hand routing preferred). The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. (Common mode current is caused by differential signals whose currents are not perfectly matched.)
- Ferrite beads and bypass caps are recommended on V_{CC} and V_{SS}, the USB power and ground lines, to minimize EMI radiation. They should be placed as close as possible to the USB connector. The capacitor values should be between 0.01 µf and 0.10 µf. The recommended value of ferrite beads is 100 ohms at 100 MHz.

Figure 3-17illustrates the recommended USB signals schematic:

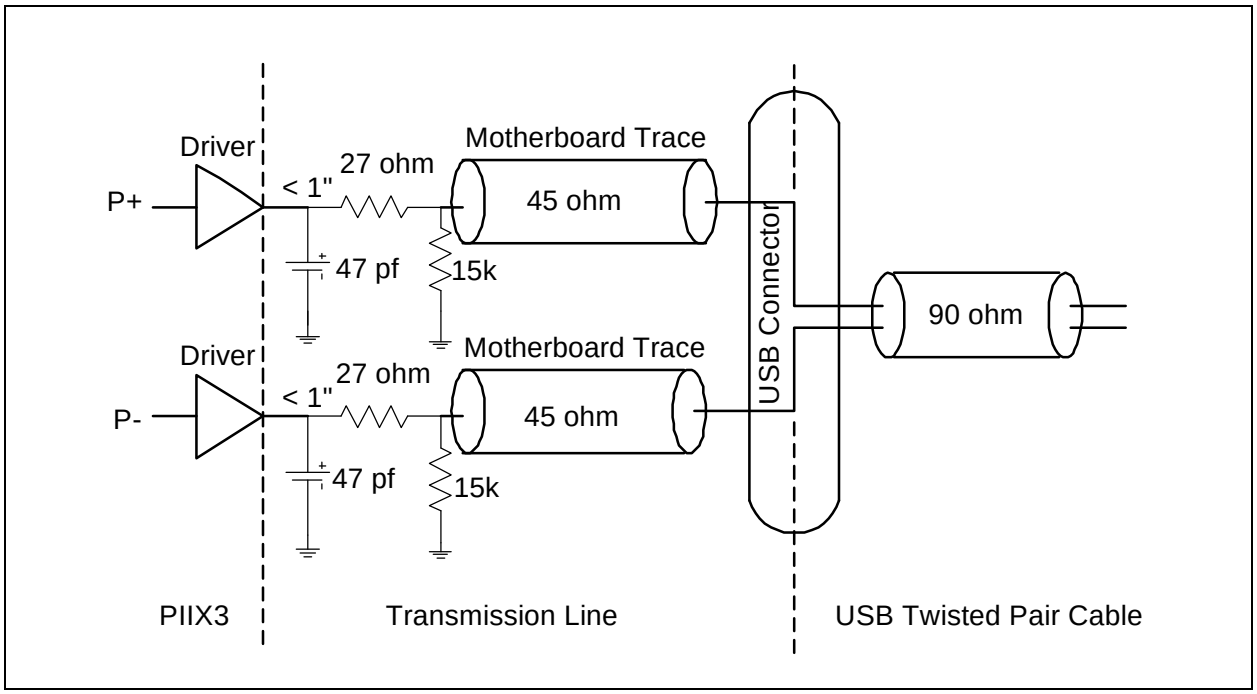


Figure 3-17. USB Data Signals

The following example illustrates a possible configuration for having a 45 ohm transmission trace. The system designer is responsible for ensuring that a particular configuration meets their requirements.

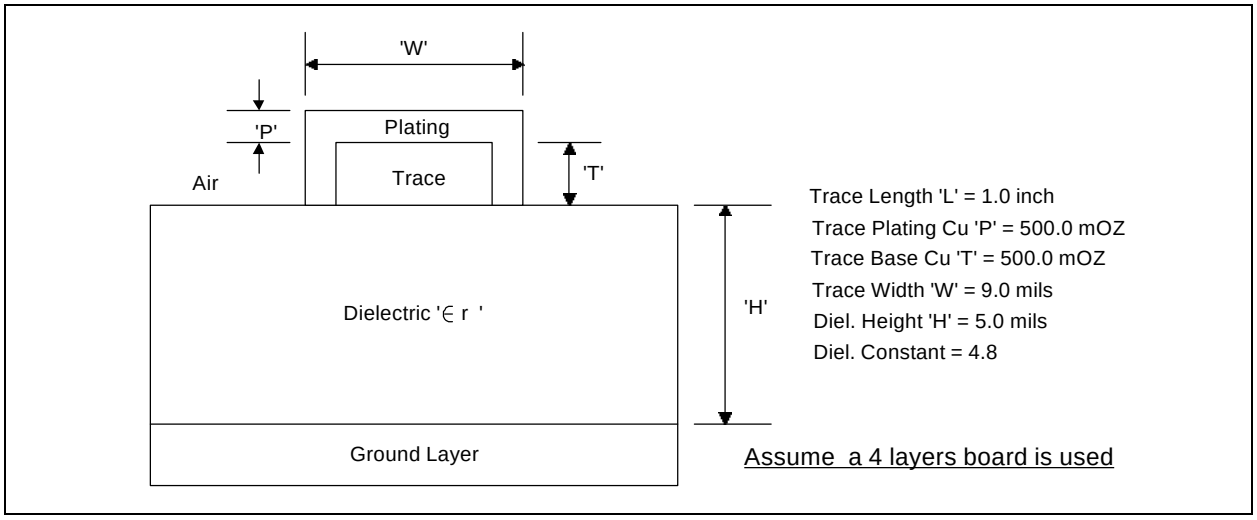


Figure 3-18. Configuration Example Using a 45 ohm transmission trace

The results of example on previous page are:

- Impedance ‘Z0’ = 45.4Ω
- Line Delay = 160.2 pSEC
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Resistance @ 20°C = 53.9 mΩ
- Trace Height = 1.4 mil

3.3.12 Options for USB Connector Implementation

There are two options recommended for attaching the USB signal and power lines to the external connector. The first is the simplest, as the connector attaches directly to the motherboard and no further design considerations are necessary. The second involves use of a printed circuit riser card to connect the USB lines from a motherboard header to a USB connector installed into a standard PC slot tab. The printed circuit riser card must be designed following the guidelines mentioned in the previous section.

A ribbon cable must not be used in place of the printed circuit riser card due to adverse effects on circuit characteristics and EMI radiation.

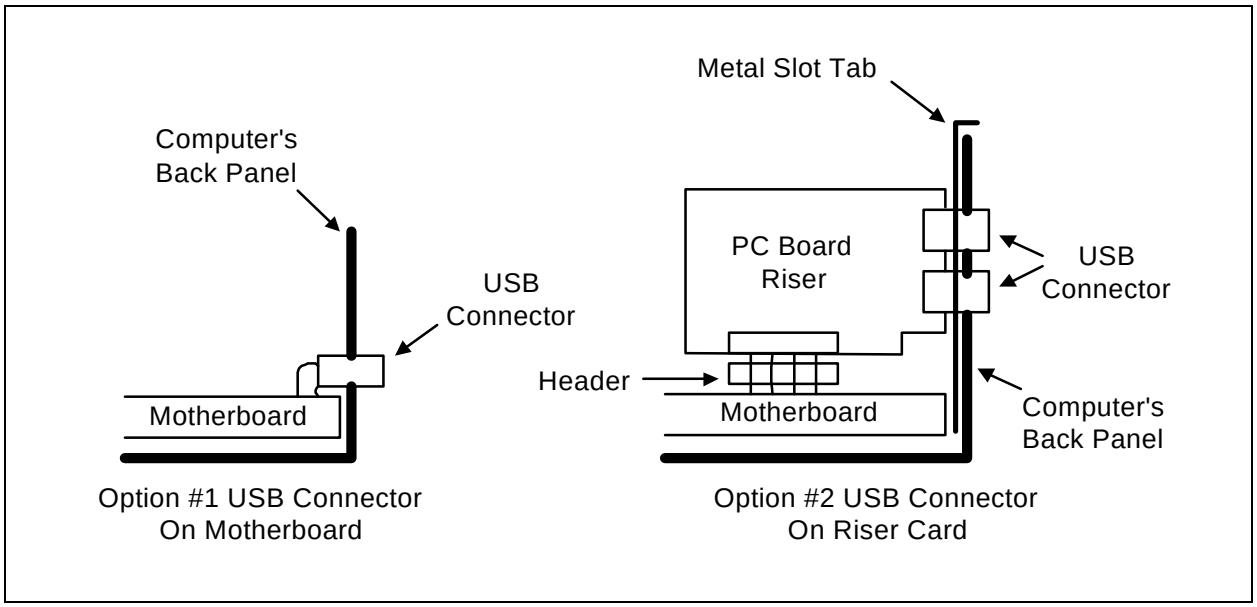


Figure 3-19. Options for USB Connector

For the printed circuit implementation, it is important that the previously described guidelines for USB signal pairs on the motherboard and the riser card are 90 ohms. Figure 3-20 shows the impedance model of USB transmission lines with use of a riser card.

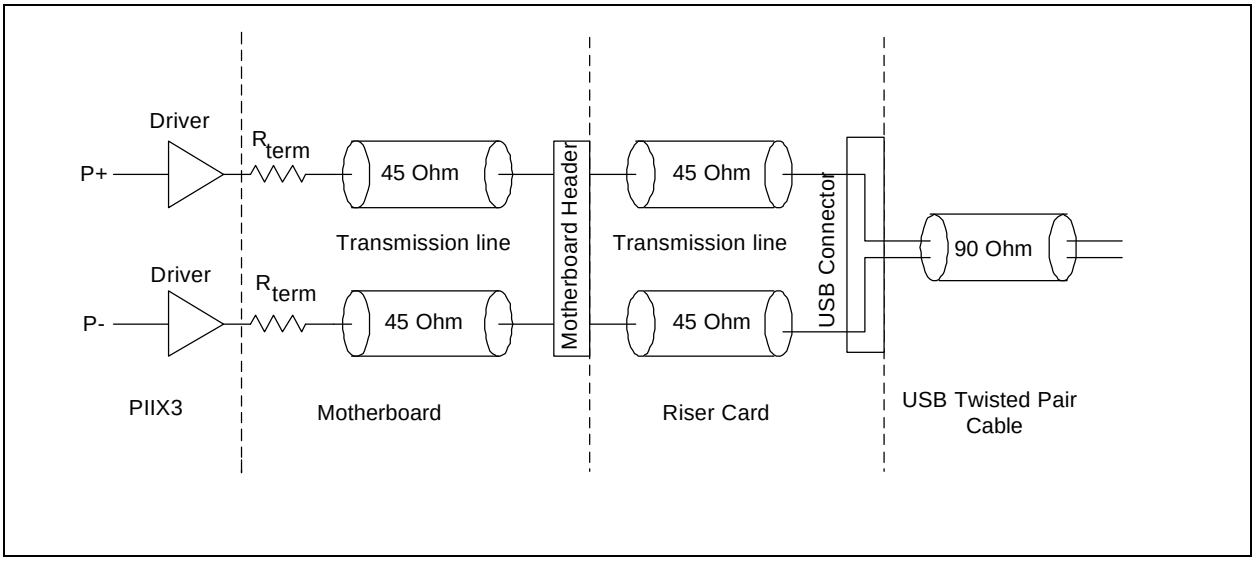


Figure 3-20. USB Data Signals with Riser Card

4

System Clock Requirements

CHAPTER 4
SYSTEM CLOCK REQUIREMENTS

This section outlines the recommended clock synthesizer specifications for an Intel 430VX PCIset (430VX) system design.Table 4-1 lists the A.C. timing requirements of the clock generation logic.

Table 4-1. AC Timing Requirements

Sym	Parameter	66 MHz		60 MHz		Units	Notes
		Min	Max	Min	Max		
tHKP	Host CLK period	15		16.7		ns	
tHKPS	Host CLK period stability		250		250	ps	1, 7
tHKH	Host CLK high time	5		5		ns	4
tHKL	Host CLK low time	5		5		ns	5
tHRISE	Host CLK rise time	0.5	2.0	0.5	2.0	ns	8
tHFALL	Host CLK fall time	0.5	2.0	0.5	2.0	ns	8
tJITTER	Host CLK Jitter		200		200	ps	
Duty Cycle	Measured at 1.5V	45	55	45	55	%	
tHSKW	Host Bus CLK Skew		250		250	ps	1
tHSTB	Host CLK Stabilization from power-up		3		3	ms	6
tPKP	PCI CLK period	30.0	∞	33.3	∞	ns	2
tPKPS	PCI CLK period stability		500		500	ps	7
tPKH	PCI CLK high time	12		13.3		ns	
tPKL	PCI CLK low time	12		13.3		ns	
tPSKW	PCI Bus CLK Skew		500		500	ps	1
tHPOFFSET	Host to PCI Clock Offset	1.0	5	1.0	4.0	ns	1, 3
tPSTB	PCI CLK Stabilization from power-up		3		3	ms	6

NOTES:

1. These signals are measured on the rising edge of adjacent CLKs at 1.5V.
2. PCI Clock is the host clock divided by two.
3. The Host CLK must always lead the PCI CLK as shown in Figure 4-3. This must be guaranteed by design under loaded conditions. This is a function of drive strength as well as routing topologies. This is a combined CLK driver requirement and a layout requirement.
4. tPKH is measured at 2.4V as shown in Figure 4-4.
5. tPKL is measured at 0.4V as shown in Figure 4-4.
6. The time specified is measured from when Vddq achieves its nominal operating level (typical condition Vddq = 3.3V) till the frequency output is stable and operating within specification.
7. Defined as once the clock is at its nominal operating frequency the adjacent period changes can not exceed the time specified.
8. tHRISE and tHFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.4V (1mA) JEDEC Specification.

4.1 PIIX3 USBCLK Requirements

This section outlines the recommended USB clock input specifications for a 82371SB PIIX3 system design. Table 4-2 lists the A.C. timing requirements of the clock generation logic.

Table 4-2. AC Timing Requirements

Sym	Parameter	48 MHz		24 MHz		Units	Notes
		Min	Max	Min	Max		
Frequency Tolerance	USB CLK Frequency Tolerance		±2500		±2500	ppm	
tUKH	USB CLK high time	7		17.5		ns	1
tUKL	USB CLK low time	7		17.5		ns	2
tURISE	USB CLK rise time		1.2		1.2	ns	3
tUFALL	USB CLK fall time		1.2		1.2	ns	3
tJITTER	USB CLK Jitter, Cycle-to-Cycle		500		500	ps	4
tJITTER, Absolute	USB CLK Jitter, Absolute		±700		±700	ps	
Duty Cycle	Measured at 1.5V	40	60	45	55	%	

NOTES:

1. tUKH is measured at 2.0V as shown in Figure 4-1.
2. tUKL is measured at 0.8V as shown in Figure 4-1.
3. tURISE and tUFALL are measured as a transition time through the threshold region Vol = 0.8V and Voh = 2.0V.
4. Frequency Tolerance needs to be taken into the consideration in a particular implementation. See USBCLK Jitter section.

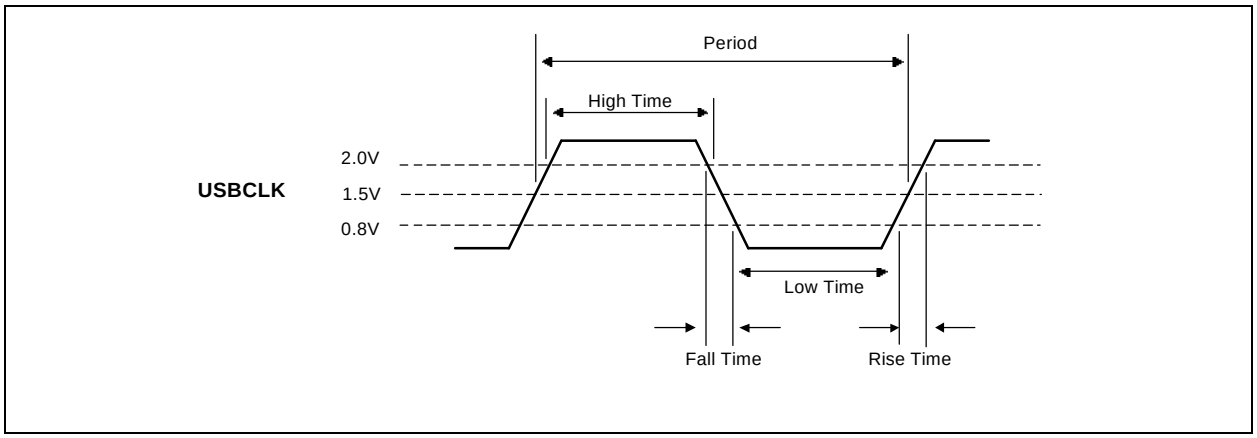


Figure 4-1. USBCLK Waveform

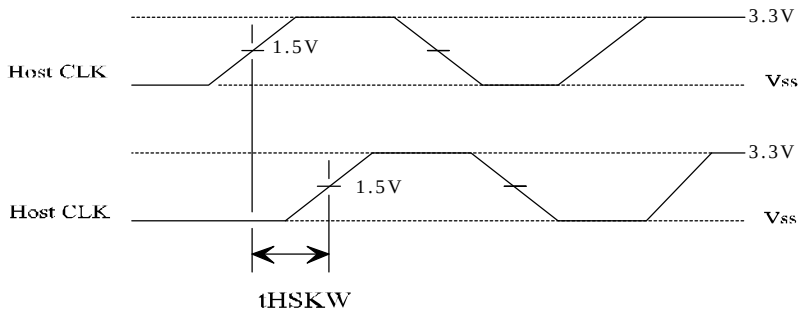


Figure 4-2. Host CLK to Host CLK Skew

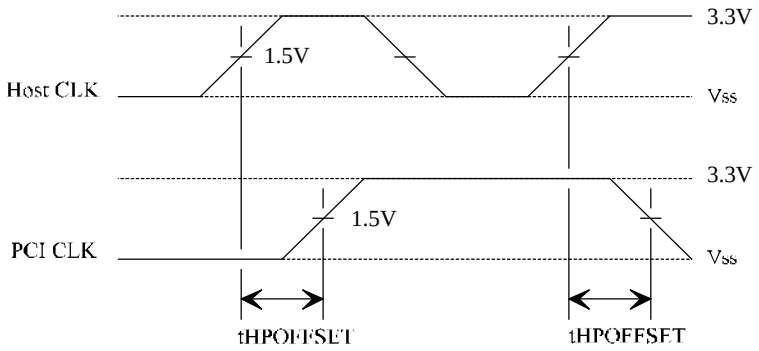


Figure 4-3. Host CLK to PCI CLK Offset

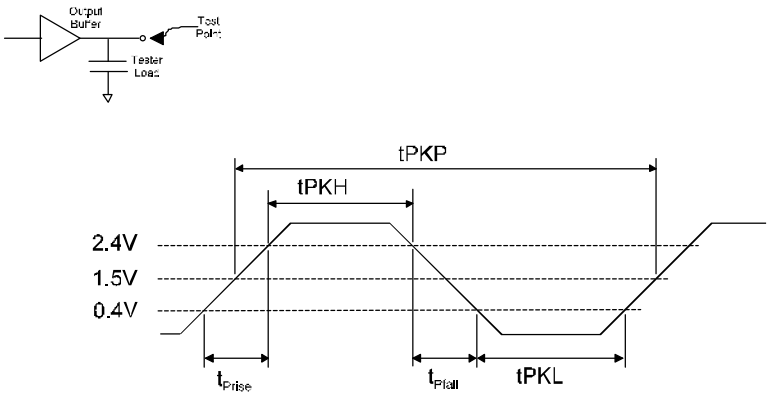


Figure 4-4. Clock Waveform

Table 4-3. Maximum Expected Capacitive Loads on Clocks

Clock	Load	Units	Notes
CPU Clocks (PCLK)	15	pF	1 or 2 loads
PCI Clocks (BCLK)	35	pF	1 slot to 2 motherboard loads
Ref0	45	pF	3 slots maximum
Ref1	30	pF	2 slots maximum
Ref2	25	pF	3 motherboard devices maximum

Table 4-4. Maximum Expected Capacitive Loads on Clocks

Clock Type	Series Resistor Value[1]	Max. Trace Length[2]	Max. Rcvr Load	Notes
48 MHz	10Ω	15”	15 pF	2 motherboard loads
24 MHz	10Ω	15”	15 pF	2 motherboard loads

NOTES:

1. A 10Ω resistor is used for 2 motherboard loads.
2. Trace length from the driver to the series resistor is assumed to a maximum of 1”.

4.2 System Considerations

The diagrams shown below are typical Clock Driver routing topologies for the 430VX platforms

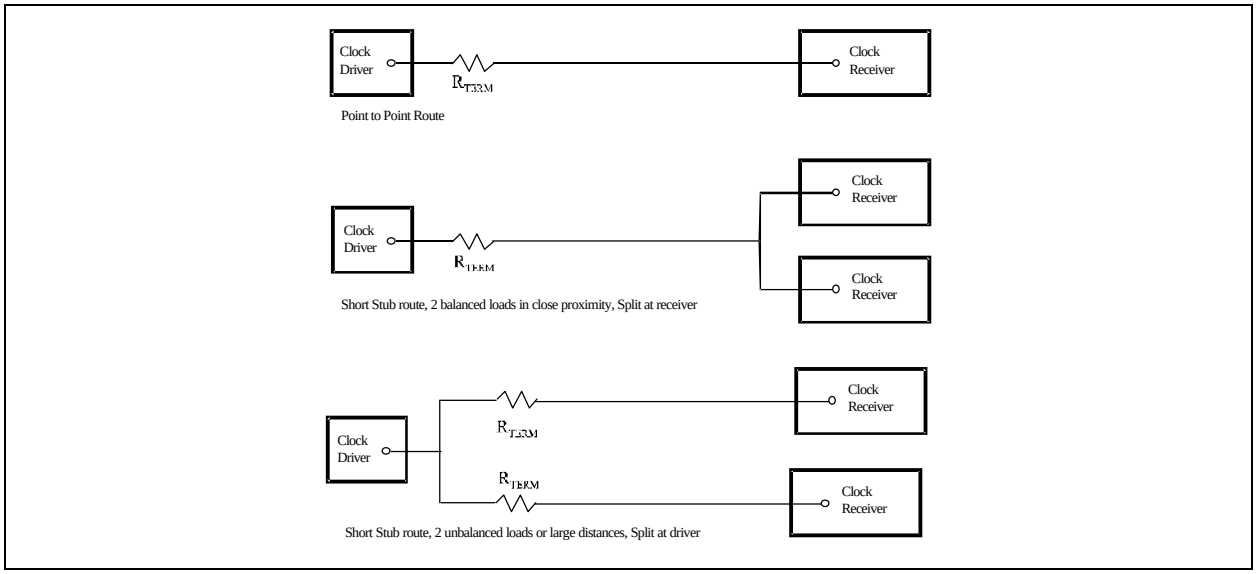


Figure 4-5. Clock Routing Topologies

NOTES:

1. Series termination resistors may be required. Selection of layout topologies and buffer drive strength will determine termination requirements (resistor values).
2. Series termination resistors should be placed as close to the driver as possible.

Table 4-5. Characteristics at Clock Destination

Symbol	Parameter	Min	Max	Units	Notes
V_{ih}	3.3V Input High Voltage	2.0	V_{DD} + .3	V	1
V_{il}	3.3V Input Low Voltage	-0.3	0.8	V	1
C_{in}	Input Pin Capacitance		6	pF	

NOTES:

1. Signal edge is required to be monatomic when transitioning through this region.

4.3 Suggested Pinout Requirements

The following section defines a generic pinout and base requirements for 430VX Reference Platform Designs. This section can also be used as an example for development of other custom clock synthesizer/driver components. This is not the only solution that can be derived. Please contact the specific clock synthesizer vendors for their respective decoupling and layout guidelines.

Features:

- Four Copies of CPU Clock @ 66.66 MHz or 60 MHz-selectable (5 Copies needed for an SMBA/non-SDRAM design)
- Six Copies of PCI Clock (Sync. CPU Clock/2)
- One copy of USB Clock @ 48 MHz (3.3V TTL)
- Three copies of Ref. Clock @14.31818 MHz
- Ref. 14.31818 MHz Xtal Oscillator Input
- Test Mode support
- Package Type SOIC: 28 pin

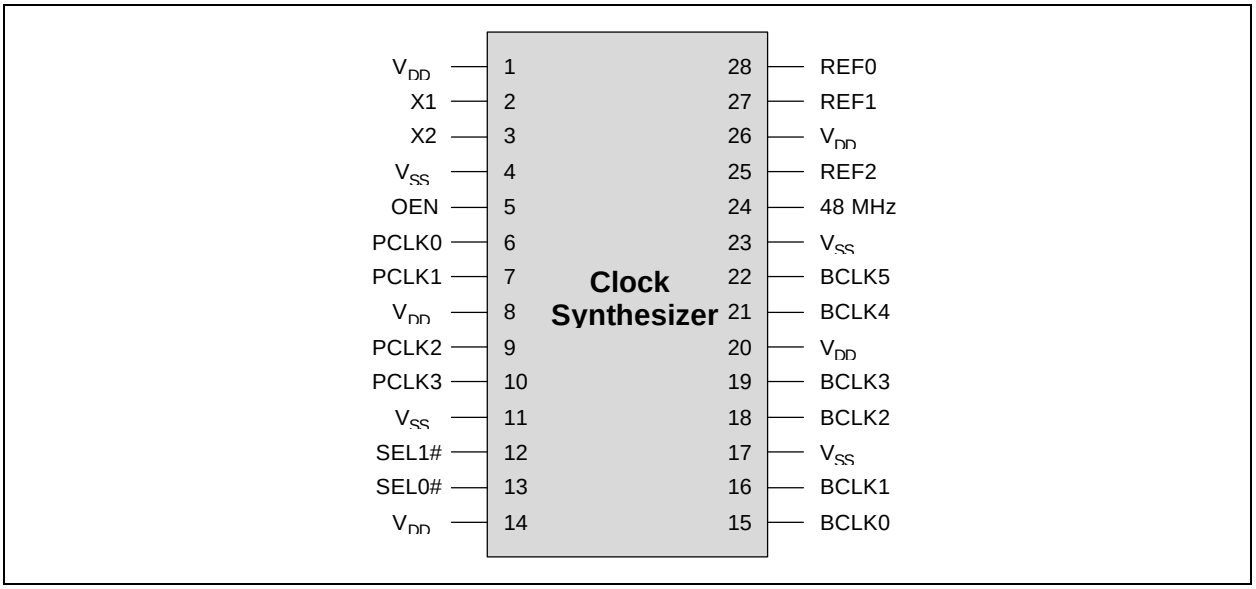


Figure 4-6. Clock Synthesizer

NOTES:

1. Pins 1 and 26 may be used as outputs for the loop filter by some clock synthesizer vendors.
2. Please refer to your clock synthesizer vendors specifications for complete details.

5

Motherboard Layout Guidelines for PIIX3 USB Implementations

CHAPTER 5
MOTHERBOARD LAYOUT GUIDELINES FOR PIIX3 USB IMPLEMENTATIONS

5.1 PIIX3 Implementation

The PIIX3 contains a Universal Serial Bus (USB) Host Controller which moves data between the main system memory and devices on the USB. The host controller also includes the root hub with two USB ports. This permits the connection of two USB peripherals or hub devices directly to the PIIX3. The PIIX3 Host Controller completely supports the standard Universal Host Controller Interface (UHCI) and takes advantage of the UHCI software drivers.

The PIIX3 fully supports the USB Specification, Revision 1.0 electrical specifications. The PIIX3 supports both full speed and low speed signalings: 12 Mbps and 1.5 Mbps, and can differentiate between full speed and low speed devices connected to its USB ports.

The key electrical requirements of USB for a motherboard design are:

- The rise and fall times of 12-Mbps data signals are 4 to 20 ns.
- The rise and fall times of 1.5-Mbps data signal are 75 to 300 ns.
- 90 ohm signal impedance for the full speed differential signal.
- Single-ended zero state on USB ports when no function is attached.
- 500 mA minimum of DC supply current for each USB port.
- The voltage supplied by host is 4.75V to 5.25V.

6

Flash Design

CHAPTER 6
FLASH DESIGN

6.1 Dual-Footprint Flash Design

New features are coming to the PC continue to increase the size of BIOS code, pushing the limits of the 1-Mbit boundary. OEMs have already converted many PC designs to 2-Mbit BIOS and higher, and more will follow.

Since it is difficult to predict when BIOS code will exceed 1 Mbit, OEMs should design motherboards to be flexible. Design in a dual-footprint on the motherboard that accepts both Intel's 1-Mbit flash chips and 2-Mbit boot block chips. This will make the 1M-to-2M transition easier by removing the need for PCB changes to accommodate higher density components.

Intel provides various layout tools to help OEMs design in the dual-footprint. These tools are available from Intel's BBS, WWW (http://www.intel.com/design/flcomp/devtools/flas4.html), and literature distribution center. Look for Application Note AP-623 "Multi-Site Layout Planning with Intel's Boot Block Flash Memory" (Order #: 292178-002). This document provides detailed information on flexible layouts.

Shown below are two of the reference layouts that Intel furnishes to customers. Layouts for plastic dip (PDIP) to TSOP and PSOP are also available. These layouts are described in AP-623 and are available electronically (Gerber and Postscript formats). Note the small amount of extra board space needed to implement the dual-footprint layouts.

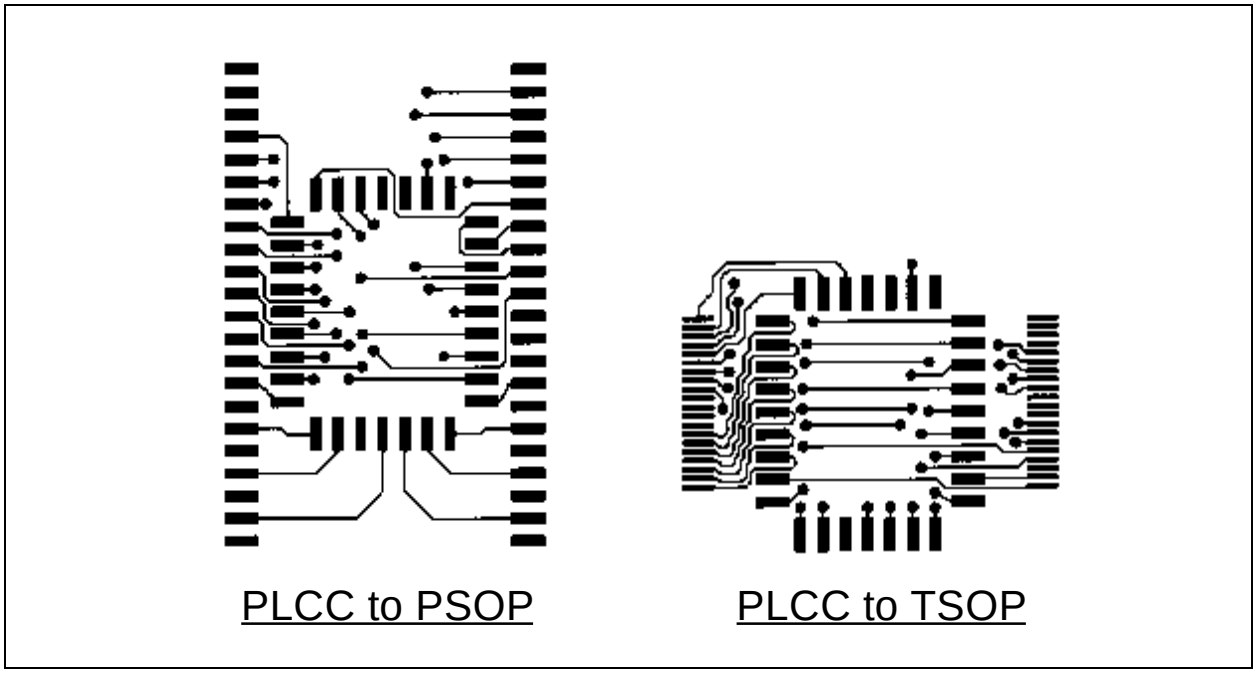


Figure 6-1. Dual-Footprint Flash Layouts

6.2 Mb Flash Design Considerations

6.2.1 Interfacing the 28F002BX FLASH (2 Mb) with the 430VX PCIset

The following design considerations must be taken into account when Intel's 28F002BX (2 Mb) Flash devices are implemented in Intel 430VX PCIset (430VX) designs. The 2-Mb Flash devices use an Address Transition Detection (ATD) mechanism to improve their performance. When interfacing Flash devices that employ the ATD mechanism, the designer needs to make sure that the address transition time is not more than 10 ns while CE# is active (low). If the address transition time is more than 10 ns invalid data can result on the data bus. When 2-Mb Flash devices are interfaced to the ISA bus they can be exposed to address transitions in excess of 10 ns. Consequently, motherboard designer's need to interface the 2-Mb Flash with the 430VX differently than the 1-Mb Flash.

The 430VX Flexible Motherboard Reference Platform currently implements the 28F001BX (1 Mb) Flash device, which does not employ the ATD circuitry. The current implementation is shown in Figure 6-2.

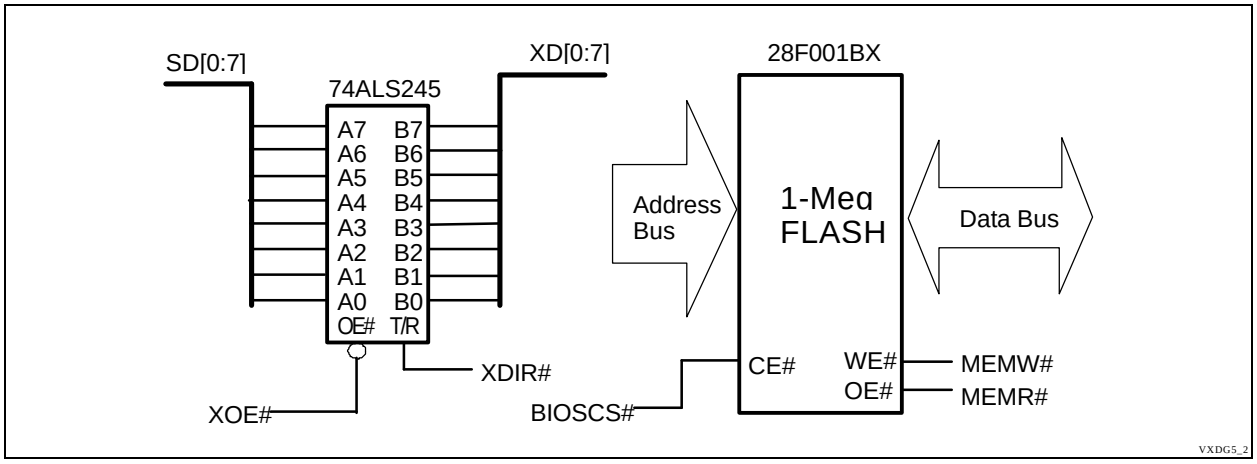


Figure 6-2. Interfacing the 1-Mbit Flash to the 430VX

For 2-Mb Flash implementations that have no other memory devices on the X-Bus, the XOE# signal can be used to drive the Flash CE# input instead of BIOSCS# (Figure 6-3). The implementation shown in Figure 6-3 ensures that the Flash device is only enabled when addresses are stable.

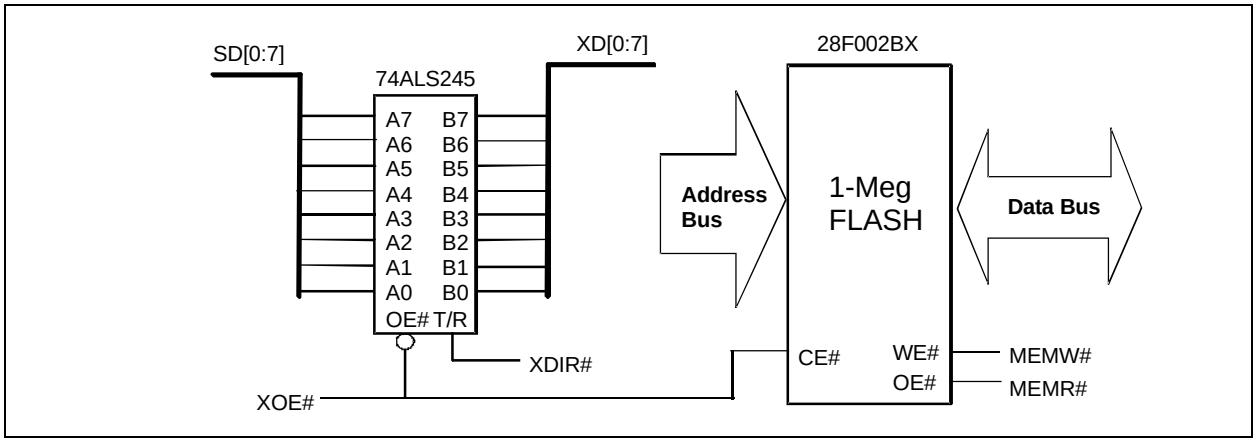


Figure 6-3. Interfacing the 28F002BX to the 430VX

If other devices are present on the X-bus, the CE# input on the Flash should be generated by OR-ing (74ALS32) XOE# with BIOSCS# as shown in Figure 6-4.

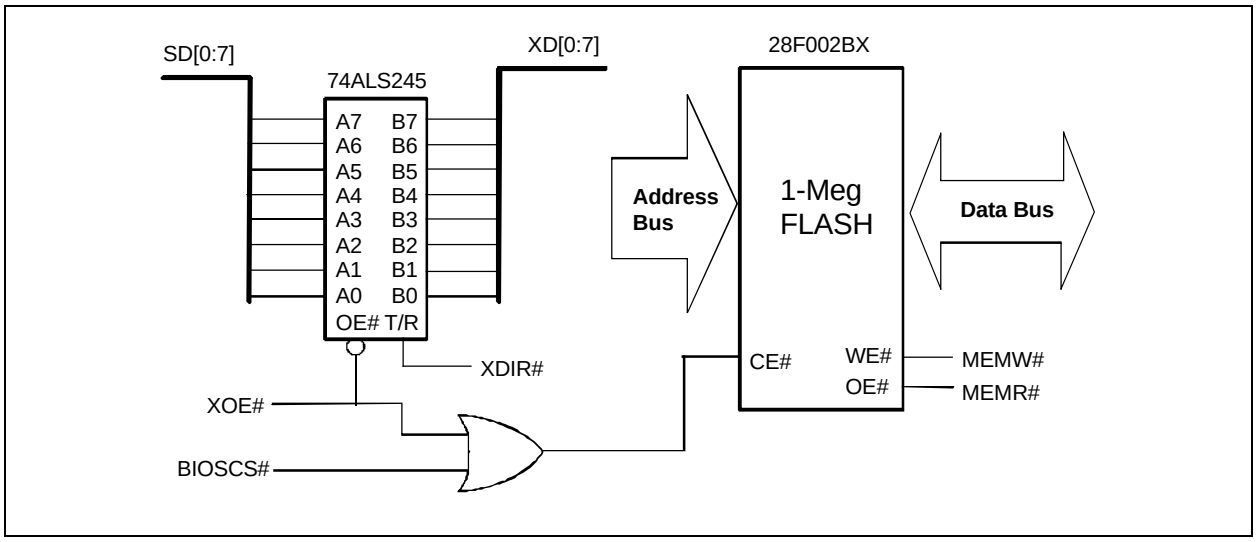


Figure 6-4. Interfacing the 28FC02BX to the 430VX when there are Other Memory Devices on the X-Bus

7

Third Party Support

CHAPTER 7
THIRD PARTY SUPPORT

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components and/or software. Please contact the manufacturer for specific information regarding performance, availability, pricing, and compatibility.

7.1 BIOS Vendors

The following BIOS vendors provide firmware to support the Pentium processor and 430VX PCIset.

Table 7-1. BIOS Vendors

Vendor	Address	Contact	Fax	Phone
AMI—American Megatrends Inc.	6145 F Northbelt Parkway Norcross, GA 30071	David Maddox	(770) 263-9381	(770) 263-8181
Award Software International	777 East Middlefield Rd. Mtn View, CA 94043	Jeffrey Flink	(415) 968-0274	(415) 968-4433
IBM Surepath	1000 NW 51st Street Boca Raton, FL 33429	David Deria	(407) 982-8978	(408) 982-0522
Phoenix	2575 McCabe Irvine, CA 92714	Jerry Ward John Archer	(714) 440-8300 (714) 440-8300	(714) 440-8017 (714) 440-8009
Systemsoft	313 Speen Street Natich, MA 01760	Karen Cummings	(508) 651-8188	(508) 651-0088

7.2 IBIS Simulation Tools

Table 7-2 lists companies committed to supporting IBIS modeling. These companies include the traditional vendors of SPICE software, as well as the new packages focused primarily at board-level interconnect simulation. Contact each vendor to find out about their IBIS offerings. See *I/O Buffer Simulation* section for additional information on IBIS.

Table 7-2. IBIS Tool Support Vendors

Company	Phone	IBIS Contact Name	Software
Anacad	+49 (731) 954-5414	Steffen Rochel	HDL-A/Eldo
Ansoft	(412) 261-3200	Henri Maramis	Maxwell SI
Cadence	(508) 262-6488	C. Kumar	DF/SigNoise
Contec Micro.	(408) 434-6767	Dileep Divekar	SI
Hyperlynx	(206) 869-2320	Kellee Crisafulli	Linesim
Incases	++49-5251-284-155	Werner Rissiek	FREACS

Company	Phone	IBIS Contact Name	Software
Integrated Silicon Systems, Inc.	(412) 832-9627	Eric Bracken	PSI Boards
Interconnectix	(503) 684-6641	Bob Ross	IS
IntuSoft	(303) 833-0710	Charles Hymowitz	IsSpice
Mentor Graphics	(408) 436-1500	Greg Doyle	SImnet
MicroSim	(714) 770-3022	Arthur Wong	PSpice
Quad Design	(805) 988-8250	Jon Powell	TLC/XTK
Quantic Labs	(204) 942-4000	Mike Ventham	Phidias
Symmetry Design Systems, Inc.	(415) 949-9600	Andy Hughes	MODPEX
UniCAD Canada Ltd.	(613) 596-9091	Stephen Lum	UniSolve
Zeelan	(503) 520-1000	George Opsahl	Models
Zuken-Redac	+44 684 294161	John Berrie	Redac

Table 7-3. List of Qualified Socket 7 Vendors

Vendor	Phone	Socket Description
Amp	(800) 522-6752	SLAZ, OC, T
Appros	(408) 567-1234	SLAZ, OC, T
Augat	(800) 999-7646	SLAZ, OC, T
Berg/McKenzie	(510) 651-2700	SLAZ, OC, T
FOXconn	(408) 749-1228	SLAZ, OC, T
JAE	(800) 523-7278	SLAZ, OC, T
Methode	(800) 323-6864	SLAZ, OC, T
Molex	(708) 527-4470	SLAZ, OC, T
Preicontact	(215) 322-3424	SLAZ, OC, T
Producer	886-2-202-3578	SLAZ, OC, T
Semtech	(805) 498-2111	SLAZ, OC, T
Yamaichi	(800) 769-0797	SLAZ, OC, T

NOTES:

1. SLAZ=Side Lever Actuated ZIF, OC=Open Center, and T=Tabs.

7.3 DRAM Cache

The following lists a DRAM Cache manufacturer providing components that can be used with the 430VX. Intel does not guarantee availability or testing of the referenced parts. Please contact the DRAM vendor and listed contact for further information.

Table 7-4. DRAM Cache Vendors

Vendor	Contact Name, Address	Phone #, FAX #
MOSYS Inc.	Gary Banta Mosys Inc. 2670 Seely Ave. San Jose, CA 95134	(408) 321-0770 FAX: (408) 321-0780

8

Customer Reference Board Schematic Overview

CHAPTER 8
CUSTOMER REFERENCE BOARD SCHEMATIC OVERVIEW

This section provides the schematics, jumper settings, component placement, and bill of materials for the Intel 430VXPCIset (430VX) customer reference board.

8.1 Schematics

Sheet 1: Title and Block Diagram

Sheet 2: Processor, Host Bus Frequency Select and Misc. Host Bus Pull-up Resistors

JB1 determines whether the CPU core frequency to host bus relationship is 2X, 3/2X, or 5/2X. The WB_WT# signal is pulled up in order to place the CPU's L1 cache in write-back mode. The signals SMI#, STPCLK#, INTR, NMI and IGNNE# are open-collector outputs from the PIIX3 (Sheet 10), and must be pulled up to 3.3V as shown. A20M# is passed through an open-collector driver and must also be pulled up to 3.3V. Parity is not supported, so PEN# and the DP[0:7] lines are pulled up.

Sheet 3: Clock Generator

For specific decoupling and layout recommendations regarding the clock generator, contact the clock generator vendor(s). Care must be given to this area or clock signal integrity issues are likely to arise.

Sheet 4: TVX

The TVX supports 4 Mbytes to 128 Mbytes of system memory with five RAS lines and also supports symmetrical and asymmetrical addressing for 512Kx32, 1Mx32, 2Mx32, and 4Mx32 deep SIMM modules (single- and double-sided). The TVX supports SDRAM 1Mx64, 2Mx64, and 4Mx64 deep DIMM modules (asymmetrical single- and double-sided). The 430VX does not support parity.

Sheet 5: TDX's

Note the Even/Odd byte lane arrangement between the two TDX's.

Sheet 6: 256-KB Pipelined Burst SRAM L2 Cache

The L2 cache is implemented using two 32Kx32 Pipelined Burst SRAMs. The data SRAMs are powered by the 3.3V plane, while the tag SRAM is powered by the 5V V_{CC} plane. The pull-up/down resistors (strapping resistors) on HA[31:28] are sampled by the TVX at reset. In this design, the TVX is configured via the strapping for 256-Kbyte Pipelined Burst SRAM.

Sheets 7 and 8: DRAM Connectors

Non-parity DRAM SIMMs are to be used. Although it is safe to use parity SIMMs, the parity function will not be used.

Sheet 9: Flash BIOS

The 82430VX Reference Board Design supports either 1-Mbit or 2-Mbit Flash devices.

Sheet 10: PIIX3

When running a 33-MHz PCI bus, J26 should be shorted in order to obtain the proper SYSCLK frequency (8.33 MHz). Designs that run the PCI bus at 25 MHz must open J26 to obtain the correct SYSCLK frequency (25 MHz/4 = 8.33 MHz). Note U4 and U3 connectivity since these transceivers are controlled by the PIIX3. These transceivers are required since the PIIX3 multiplexes DD[15:0] with SA[19:8], SBHE#, APICCS# and PCS# signals.

Sheet 11: IDE Connectors

The 74ALS245s are used to create the SA[8:19], SBHE#, and PCS# signals. Note that the PCS# signal is not used in this design, but is simply pulled up. Two IDE connectors are supported, each supporting two devices. Note the series terminating resistors on many of the IDE signals. Note: Some older drives do not support both chipselects be asserted. To support these older drives the chipselects are generated by NANDing SOE# and the appropriate LA signal (i.e., CS1P# is generated by NANDing SOE# and LA21).

Sheet 12: Ultra I/O Controller

The I/O controller incorporates the Floppy disk controller, Serial and Parallel ports, Real-time clock and keyboard Controller.

Sheet 13: USB interface, Floppy and Communication Port Connectors

Refer to the USB Layout and Routing guidelines section of this document to obtain important layout considerations for the USB interface.

Sheet 14: Parallel Port Interface

Sheet 15: Keyboard and Mouse Connectors

Sheet 16: SMBA Graphics Controller

Sheet 17: Video Connectors

Sheet 18: Power, Speaker, and Hard Disk LED Connectors

When the Pentium Processor (735/90, 815/100) is used, the 3.3V connector will not be connected. The 3.3V required by the processor, PCIset, and L2 cache will be provided by the on board Voltage Regulator.

Sheets 19 and 20: PCI Connectors

The 82430VX PCIset supports up to 4 PCI slots. This design implements three slots since the SMBA interface uses one REQ#/GNT# pair.

Sheets 21 and 22: ISA Connectors

The 82430VXPCIset supports up to five ISA slots. This design implements three slots.

Sheet 23: Various PCI and ISA Pull-Up/Pull-Down resistors

Sheet 24: Voltage Regulator

Sheet 25: Spare Gates

Sheet 26: Decoupling Caps

8.1.1 Design Example—Interfacing SDRAM to the 82430VX PCIset

The 430VX motherboard design described in this document does not support SDRAM. However, this section provides an example of an SDRAM implementation using the 430VX.

Sheet 1: Clock Generator

Sheet 2: DIMM Connectors
Sheet 2 shows the DIMM interface.

Sheet 3: TVX Interface
Sheet 3 shows the interface between the TVX and SDRAM.

8.2 Jumpers

This section contains jumper settings for 430VX Customer Reference Board.

8.3 Component Placement

This section shows the component placement for 430VX Customer Reference Board.

8.4 Bill of Materials

This section contains a Bill Of Materials (BOM) for the 430VX Customer Reference Board.

Table 8-1. Bill Of Materials

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
1N4148SOT23	SOT23	Diode, 1N4148	2	Diodes Inc.	IMBD4148	D1, D3
1N5817	TH	Diode, 1N5817	1	Motorola	1N5817	D2
28F001BX-T150	DIP32	Flash Mem., 1 Mbit, w/boot block, 150 nS	1	ITL	P28F001BX-T150	U7
2N3904SOT23	SOT23	3904 Transistor	1	National Semiconductor	MMBT3904	Q2
32KX32PBSRMPTQ-8	QFP100	32Kx32 Pipelined Burst SRAM, 8 ns	2	ISSI	IS61C632-8TQ	U28, U29
32KX8SRAMSN-15	SOJ28	32Kx8 SRAM (15 ns)	1	ISSI	IS61C256AH-15J	U19
6270B	TH	Heat Sink, Horizontal Mount for T0-220	1	THRM	6270B	Q1
7407S	SOIC14	IC, Hex buffer, open collector	2	Texas Instruments	SN7407D	U16, U27
74ALS00S	SOIC14	IC, Quadruple 2-input NAND gate	1	NSC	DM74ALS00AM	U1
74ALS08S	SOIC14	IC, Quadruple 2-input AND gate	1	NSC	DM74ALS08M	U2
74ALS245S	SOIC20	IC, Octal tristate transceiver	2	NSC	DM74ALS245AWMX	U3, U4
74ALS32S	SOIC14	IC, Quadruple 2-input or gate	1	NSC	DM74ALS32M	U15
74HCT14S	SOIC14	IC, Hex Schmitt trigger inverters	1	HRS	CD74HCT14M96	U14
74LS125S	SOIC14	IC, Quadruple tristate buffer	2	Motorola	SN74LS125ADR2	U17, U18
82371SB	PQFP208	Triton PCI ISA/IDE Accelerator III	1	ITL	SB82371SB	U12
82437VX	PQFP208	Triton VX System Controller	1	ITL	S82437VX	U13
82438VX	PQFP100	Triton VX Data Path	2	ITL	S82438VX	U11, U20
BT1225C2H	TH	Battery, 3V lithium, 12.5 mm dia. coin cell, 2 tab	1	RAYO	BR1225T2B	BT1
C100CS00EC	SM0603	Cap., cer., 10 pF, 25V, 5%	2	AVX	06033A100JAT2	C205, C206
C101CS00ED	SM0603	Cap., cer., 100 pF, 25V, 10%	16	AVX	06033A101KAT2A	C22, C26, C27, C37, C40, C43, C44, C49, C51, C55, C61, C64, C65, C68, C81, C82

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
C102CS00EE	SM0603	Cap., cer., 0.001 µF, 25V, 20%	12	AVX	06033C102MAT2A	C78, C101, C112, C115, C135, C138, C144, C170, C194, C197, C240, C256
C103CS00EM	SM0603	Cap., cer., 0.01 µF, 25V, +80%/-20%	29	AVX	06033E103ZAT2A	C5, C7, C75, C80, C83, C87, C99, C107, C108, C122, C124, C126, C127, C137, C142, C147, C151, C156, C165, C169, C175, C182, C184, C186, C192, C214, C219, C255, C257
C104CS00EM	SM0603	Cap., cer., 0.1 µF, 25V, +80/-20%	38	AVX	06033G104ZAT2A	C1, C2, C3, C4, C6, C14, C23, C28, C52, C53, C56, C57, C58, C69, C70, C71, C72, C73, C74, C79, C88, C90, C91, C92, C93, C94, C95, C100, C102, C103, C104, C105, C110, C111, C113, C114, C116, C119
C104CS00EM	SM0603	Cap., cer., 0.1 µF, 25V, +80/-20%	34	AVX	06033G104ZAT2A	C120, C121, C123, C125, C129, C130, C131, C133, C136, C139, C140, C141, C143, C145, C146, C148, C153, C154, C155, C157, C158, C159, C164, C166, C171, C172, C173, C174, C176, C177, C179, C180, C181, C183

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
C104CS00EM	SM0603	Cap., cer., 0.1 µF, 25V, +80/-20%	21	AVX	06033G104ZAT2A	C185, C187, C188, C189, C195, C196, C198, C200, C201, C203, C207, C208, C211, C218, C220, C225, C227, C245, C250, C254, C259
C104CS01EM	SM0805	Cap., cer., 0.1 µF, 25V, +80/-20%	1	AVX	08053E104ZATNA	C204
C105CS02DM	SM1206	Cap., cer., 1.0 µF, 16V, +80/-20%	1	NIC	NMC1206Z5U105M16VTR	C132
C105CS02DM-X7R	SM1206	Cap., cer., 1.0 µF, 16V, +80/-20%, X7R	18	TDK	CC1206CX7R105	C215, C216, C217, C221, C224, C228, C229, C230, C231, C232, C237, C238, C239, C246, C249, C251, C252, C253
C106ES09DE	SM4mm	Cap., elec., 10 µF, 16V, 20%	19	Panasonic	ECEV1CA100 R	C24, C38, C41, C46, C62, C84, C85, C98, C117, C118, C149, C150, C152, C167, C178, C190, C191, C213, C235
C106ES11DE	SM5mm	Cap., elec., 10 µF, 16V, 20%	2	Panasonic	ECEV1CA100 R	C45, C66
C106TS03CE	SM6032	Cap., tant., 10 µF, 10V, 20%	3	AVX	TAJC106M010AS	C96, C97, C128
C107TS05CE-LE	SM7343H	Cap., tant., 100 µF, 10V, 20%, .125 ESR	9	SPRG	593D107X0010D2	C134, C193, C202, C212, C222, C223, C236, C247, C248
C150CS00ED	SM0603	Cap., cer., 15 pF, 25V, 10%	6	AVX	06033A150KAT2A	C8, C9, C17, C30, C31, C32
C181CS00ED	SM0603	Cap., cer., 180 pF, 25V, 10%	17	AVX	06033A181KAT2A	C11, C19, C20, C21, C25, C35, C36, C39, C42, C47, C48, C50, C54, C59, C60, C63, C67
C220CS00EC	SM0603	Cap., cer., 22 pF, 25V, 5%	2	AVX	06033A200JAT2	C106, C109
C221CS00ED	SM0603	Cap., cer., 220 pF, 25V, 10%	2	AVX	06033A221KAT2A	C33, C34

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
C470CS00ED	SM0603	Cap., cer., 47 pF, 25V, 10%	6	AVX	06033A470KAT2A	C10, C18, C160, C161, C162, C163
C471CS00EE	SM0603	Cap., cer., 470 pF, 25V, 20%	11	AVX	06033C471MAT2A	C12, C13, C15, C16, C76, C77, C86, C89, C226, C233, C234
C472CS00EE	SM0603	Cap., cer., 0.0047 µF, 25V, 20%	1	AVX	06033C472MAT2A	C168
CL-GD54UM36	QFP208	Cirrus Logic VGA Graphics Controller	1	Cirrus Logic	CL-GD54UM36	U10
CN120ED05B	TH	Conn., 120 pin, PCI	3	Burndy	CEE2X60S-V3Z14W (PL)	J14, J15, J16
CN15DBFPT10B	TH	Conn., 15 pin, female d-shell, three row	1	Foxconn	DV11202-S3	J6
CN16BGD10B	TH	Conn., 8x2 pin header	1	AMP	102973-8	J19
CN26BGD10B	TH	Conn., 13x2 pin header	1	AMP	1-102973-3	J13
CN6FLU15C	TH	Conn., 6 pin, AT power plug	3	Burndy	GTC6R-1	J12, J18, J23
CN6MDF10B	TH	Single PS2 style keyboard ms connector	2	AMP	749266-1	J4, J5
CN98ED10B	TH	Conn., 98 pin card edge	3	AMP	176139-3	J9, J10, J11
CNK25BGD10BA	TH	Conn., 13x2 pin header; key pin 26	1	AMP	103675-6	J7
CNK33SH10B	TH	Conn., 17x2 pin header; key pin 5, shrouded	1	AMP	146178-2	J24
CNK39SH10B	TH	Conn., 20x2 pin header; key pin 20, shrouded	2	AMP	146178-4	J21, J22
CNK3BGS10B	TH	Conn., 4x1 pin header; key pin 2	1	AMP	104878-3	J33
CNK3BGS10BA	TH	Conn., 4x1 pin header; key pin 3	2	AMP	1031854	J20, J29
CNK4BGS10B	TH	Conn., 5x1 pin header; key pin 2	1	AMP	103185-5	J34
CNK9BGD10B	TH	Conn., 5x2 pin header; key pin 10	2	AMP	103675-5	J8, J17
FBS01K	SM0805	Ferrite bead (ACT material K)	6	ACT	KCB-0805	L2, L3, L4, L5, L12, L13
FBS01L	SM0805	Ferrite bead (ACT material L)	2	ACT	LCB-0805	L1, L15

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
FBS04B	SM1812	Ferrite bead (ACT material B)	8	ACT	CB1812/B	L6, L7, L8, L14, L16, L17, L18, L19
FDC37C935	QFP160	SMC Ultra I/O Controller, w/Phoenix K.B. BIOS	1	SMC	FDC37C935	U9
FUSEP1253S09D	SM9466	Poly Fuse 1.25A hold, 15V	3	Raychem Corp.	SMD125-2	F2, F3, F4
GD75232SOP	SOP20	RS 232 Transceiver 5 receivers, 3 drivers	2	LGS	GD75232D	U5, U8
ICS9159-02S	SOIC28	Clock Generator, ICS9159-02	1	ICS	ICS9159-02W	U25
insilpad-TO220	TO-220	Silicone insulator w/ thermally conductive filters	1	AVD	188858F00000	Q1
JB3	TH	3x2 pin header connector	1	AMP	103186-3	JB1
JP2	TH	2x1 pin header connector	4	AMP	103185-2	J26, J27, J35, J36
JP3	TH	3x1 pin header connector	7	AMP	103185-3	J1, J2, J3, J28, J30, J31, J32
L152S06D	SM1210	1.5 µH SMT inductor	1	ACT	IC210-1R5K	L20
L181S06E	SM1210	180 nH SMT inductor	3	ACT	IC1210R18M	L9, L10, L11
locknut-4-40	HDWR	4-40 Locknut	1	ITW	511-0418-00-00	Q1
LT1431CS	SOIC8	Regulator, Adjustable Shunt, .4%	1	LTC	LT1431CS8	Q1
LT1584CTO220	TO220	Regulator, positive fast response	1	LTC	LT1584CT	U30
PCB		Printed Circuit Board	1		CUSTOMER/ CM SPECIFIED	PCB1
R0000CS00SC	SM0603	Res., 0, 5%, 1/16W	7	Dale	CRCW06030R0JRT 1	R2, R6, R7, R19, R81, R106, R127
R0100CS00SC	SM0603	Res., 10, 5%, 1/16W	13	Dale	CRCW0603100JRT1	R44, R49, R50, R51, R52, R53, R55, R56, R57, R58, R59, R60, R61
R0220CS00SC	SM0603	Res., 22, 5%, 1/16W	26	Dale	CRCW0603220JRT1	R45, R67, R68, R69, R70, R71, R72, R73, R74, R75, R83, R88, R97, R98, R99, R100, R101, R102, R103, R104, R105, R114, R115, R116, R117, R118

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
R0300CS00SC	SM0603	Res., 30, 5%, 1/16W	4	Dale	CRCW0603300JRT1	R24, R26, R30, R33
R0330CS00SC	SM0603	Res., 33, 5%, 1/16W	7	Dale	CRCW0603330JRT1	R11, R12, R21, R22, R39, R42, R85
R0470CS00SC	SM0603	Res., 47, 5%, 1/16W	4	Dale	CRCW0603470JRT1	R62, R63, R64, R66
R0680CS01EC	SM1206	Res., 68, 5%, 1/8W	2	Dale	CRCW1206-680JRT5/JRT2	R134, R135
R0750CS00SC	SM0603	Res., 75, 5%, 1/16W	3	Dale	CRCW0603750JRT1	R8, R9, R10
R1000CS00SC	SM0603	Res., 100, 5%, 1/16W	2	Dale	CRCW0603-101JRT1	R65, R146
R1001CS00SC	SM0603	Res., 1K, 5%, 1/16W	11	Dale	CRCW0603102JRT1	R3, R4, R14, R15, R16, R20, R43, R77, R110, R111, R128
R1002CS00SC	SM0603	Res., 10K, 5%, 1/16W	7	Dale	CRCW0603103JRT1	R18, R48, R54, R82, R86, R87, R108
R1004CS00SC	SM0603	Res., 1M, 5%, 1/16W	1	KOA	RM73B1J105J	R46
R1350CS00SC	SM0603	Res., 135, 5%, 1/16W	1	Dale	CRCW0603-101JRT1	R40
R1502CS00SC	SM0603	Res., 15K, 5%, 1/16W	4	Dale	CRCW0603153JRT1	R23, R27, R29, R31
R1800CS00SC	SM0603	Res., 180, 5%, 1/16W	4	Dale	CRCW0603-181JRT1	R149, R150, R151, R152
R2002MS03TA	SM0805	Res., 20.0K, 1%, 1/10W	1	Dale	CRCW08052002FRT1	R113
R2200CS00SC	SM0603	Res., 220, 5%, 1/16W	11	Dale	CRCW0603221JRT1	R32, R34, R35, R47, R84, R94, R96, R121, R122, R126, R143
R2741MS03TZ	SM0805	Res., 2.74K, 0.1%, 1/10W	1	Dale	TNPW-08052741BT-9	R112
R3300CS00SC	SM0603	Res., 330, 5%, 1/16W	5	Dale	CRCW0603331JRT1	R107, R109, R123, R132, R140
R4701CS00SC	SM0603	Res., 4.7K, 5%, 1/16W	12	Dale	CRCW0603472JRT1	R5, R89, R90, R92, R93, R120, R124, R131, R141, R142, R147, R148
R5601CS00SC	SM0603	Res., 5.6K, 5%, 1/16W	2	Dale	CRCW0603562JRT1	R78, R79
R6801CS00SC	SM0603	Res., 6.8K, 5%, 1/16W	2	Dale	CRCW0603682JRT1	R37, R38

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
R8201CS00SC	SM0603	Res., 8.2K, 5%, 1/16W	1	Dale	CRCW0603822JRT1	R1
R9650MS03TZ	SM0805	Res., 965, 0.1%, 1/10W	1	Dale	TNPW-0805965BT-9	R130
RI100S09SC	SM3216	Res. Block., 10x4, iso., 5%, 1/16W	3	Rohm	MNR14E0AJ-100	RP63, RP65, RP68
RI102S09SC	SM3216	Res. Block., 1Kx4, iso., 5%, 1/16W	7	Rohm	MNR14E0AJ-102	RP2, RP4, RP7, RP10, RP11, RP15, RP72
RI103S09SC	SM3216	Res. Block., 10Kx4, iso., 5%, 1/16W	26	Rohm	MNR14E0AJ-103	RP1, RP5, RP8, RP9, RP14, RP16, RP19, RP20, RP22, RP26, RP30, RP33, RP36, RP45, RP46, RP48, RP49, RP50, RP51, RP55, RP58, RP60, RP61, RP64, RP66, RP73
RI220S09SC	SM3216	Res. Block., 22x4, iso., 5%, 1/16W	10	Rohm	MNR14E0AJ-220	RP27, RP31, RP32, RP35, RP37, RP38, RP39, RP40, RP44, RP47
RI272S09SC	SM3216	Res. Block., 2.7Kx4, iso., 5%, 1/16W	7	Rohm	MNR14E0AJ-272	RP13, RP17, RP28, RP34, RP42, RP43, RP54
RI330S09SC	SM3216	Res. Block., 33x4, iso., 5%, 1/16W	8	Rohm	MNR14E0AJ-330	RP3, RP6, RP12, RP21, RP52, RP53, RP57, RP59
RI331S09SC	SM3216	Res. Block., 330x4, iso., 5%, 1/16W	2	Rohm	MNR14E0AJ-331	RP41, RP62
RI472S09SC	SM3216	Res. Block., 4.7Kx4, iso., 5%, 1/16W	9	Rohm	MNR14E0AJ-472	RP23, RP24, RP25, RP29, RP67, RP69, RP70, RP71, RP74
RI562S09SC	SM3216	Res. Block., 5.6Kx4, iso., 5%, 1/16W	2	Rohm	MNR14E0AJ-562	RP18, RP56
screw-4-40-.33	HDWR	4-40 Panhead Screw, 1/3"	1	Century	CF1979	Q1
SHUNTS		Jumper shunts	7	AMP	382811-6	J1, J2, J3, J28, J30, J31, J32
SK321PGAZIF	PGA321	ZIF Socket for Pentium® (socket 7)	1	AMP	916637-3	U26
SK32D6	DIP32	Socket, 32 pin, DIP, .6" spacing	1	Foxconn	PA01160-T	U7

Part Number	Package Type	Description	Qty	Vendor	Vendor I.D. Number	Ref. Des.
SK72SIMVML	TH	Socket, 2Mx36 SIMM, single, vert., ml	4	AMP	822021-4	U21, U22, U23, U24
Y14318186B2E-18	TH	Xtal, 14.31818 MHz, 49-U pkg, 18 pF, 20 ppm	1	ECL	EC143-14.31818	Y2
Y32768003B2F-12	TH	Xtal, 32.768 KHz, 12.5 pF, 20 ppm	1	ECL	EC38T	Y1